

# Compal Confidential

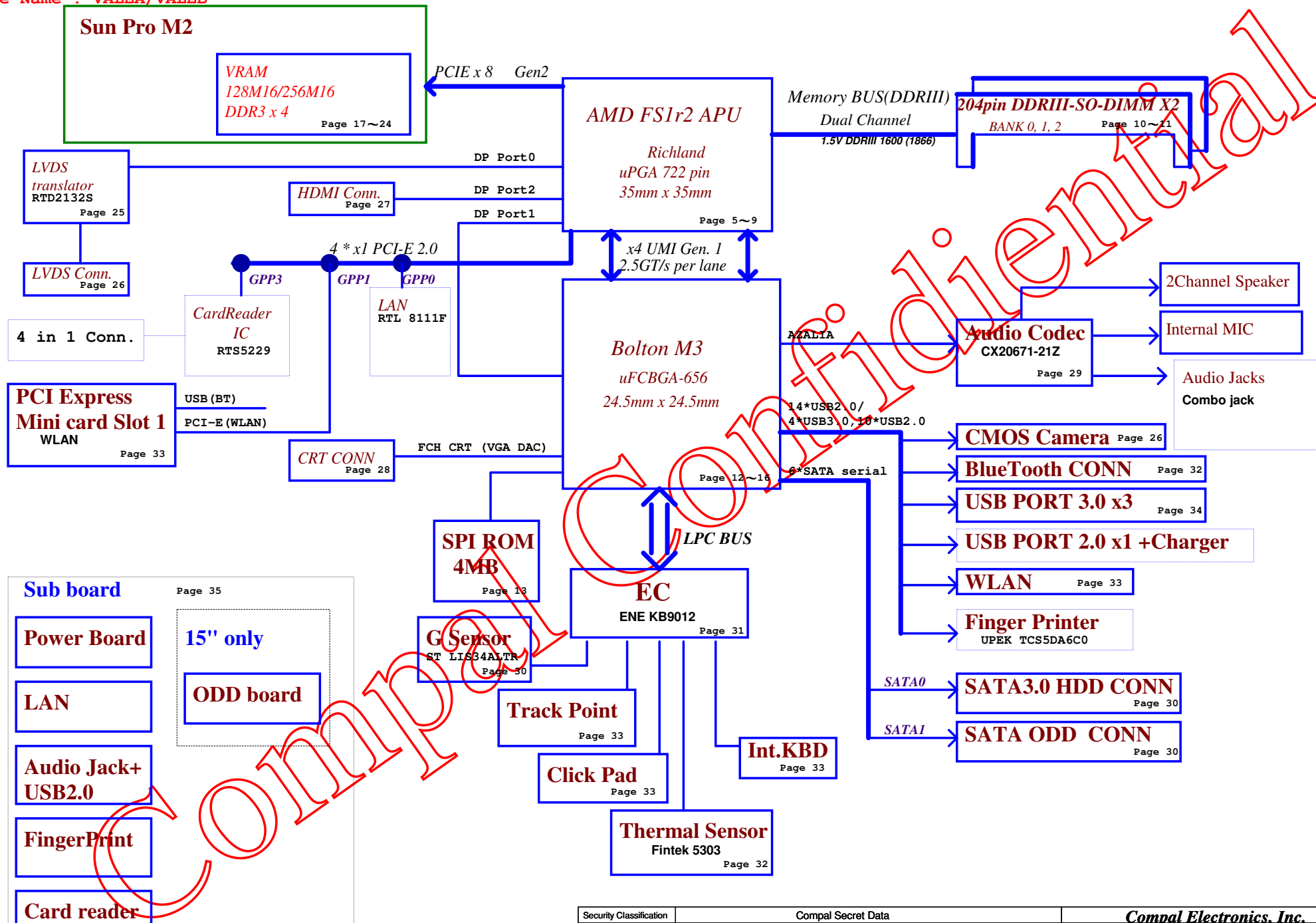
## VALEA/VALEB Schematics Document

AMD APU Richland FS1r2 + FCH Bolton-M3 + GPU Sun Pro M2

2012-11-22

REV: 1.0

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	Cover Page
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				LA-8127P	1.0
				Date	Tuesday, March 12, 2013
				Sheet	1 of 51



Voltage Rails

Power Plane	Description	S0	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for APU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+1.5V	1.5V power rail for APU VDDIO and DDR	ON	ON	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	OFF	OFF
+1.2VS	1.2V (VDDR, VDDP) switched power rail for APU	ON	OFF	OFF
+2.5VS	2.5V for APU VDDA	ON	OFF	OFF
+1.1VALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.5VS	1.5V switched power rail	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+1.5VGS	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+0.95VGS	0.95V switched power rail for VGA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS_WLAN	3.3V power rail for WLAN	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001-011xb	15H	F75303 (DDR,VRAM,CPUCORE)	1001-101xb	9AH
			SB-TSI	1001-100xb	98H
			Sun Pro M2	1000-0010b	82H
			LVDS translator		

FCH SMB0		
Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		
Security ROM		

Stencil Memo

FCH Hudson-M2/3 SATA Port List	
SATA0	HDD
SATA1	ODD
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

Comal PCIE Port List		
APU	PCIE0	LAN
	PCIE1	WLAN
	PCIE2	NC
	PCIE3	Card Reader
FCH	PCIE0	NC
	PCIE1	NC
	PCIE2	NC
	PCIE3	NC

FCH Hudson-M2/3 USB Port List	
USB1.1	
Port0	NC
Port1	NC
USB2.0	
Port0	USB2.0 Port
Port1	NC
Port2	NC
Port3	NC
Port4	NC
Port5	WLAN
Port6	CMOS
Port7	FP
Port8	BT
Port9	NC
Port10	USB 3.0
Port11	USB 3.0
Port12	USB 3.0
Port13	NC

BOM Structure

UMA@ : UMA Only  
DIS@ : DIS muxless  
CMOS@ : USB camera  
CONN@ : ME components  
X76@, H1G@, S1G@ : VRAM

BOM option and stencil

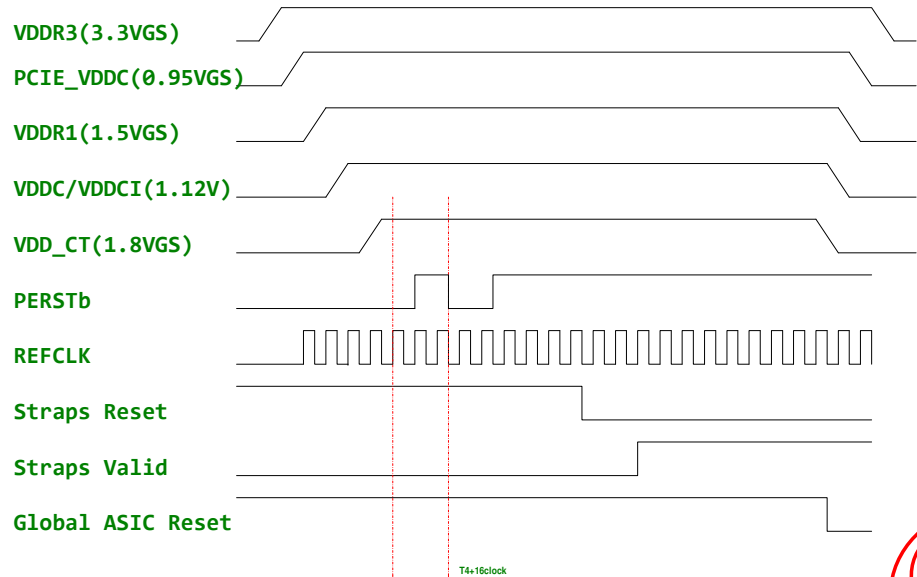
SDV:  
CMOS@/DIS@ + X76@

PJ201, PJ401, PJ502, PJ503, PJ504, PJ601, PJ603, PJ604,  
PJ701, PJ702, PJ703, PJ704, J1, J2301, J2401, J2402, J2403  
PJ402, PJ403, PJ501, PJ602, PJ801, PJ802, PJ803, PJ805

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				Customer	LA-8127P
				Date	Tuesday, March 12, 2013
				Sheet	3 of 51
				Rev	1.0

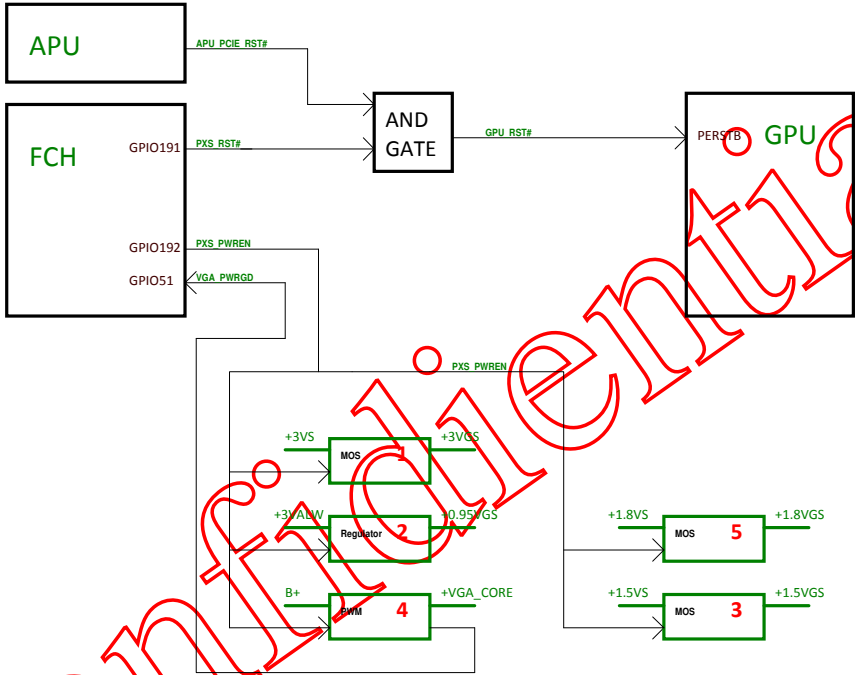
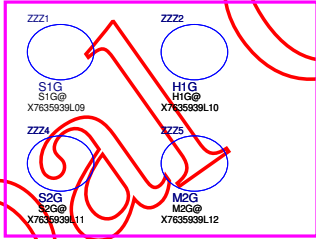
Power-Up/Down Sequence

- All the ASIC supplies, except for VDDR3, must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. There is no timing requirement on the ramp up of VDDR3 relative to other power rails.
- The external pull-up resistors on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
- VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



SUN PRO VRAM STRAP

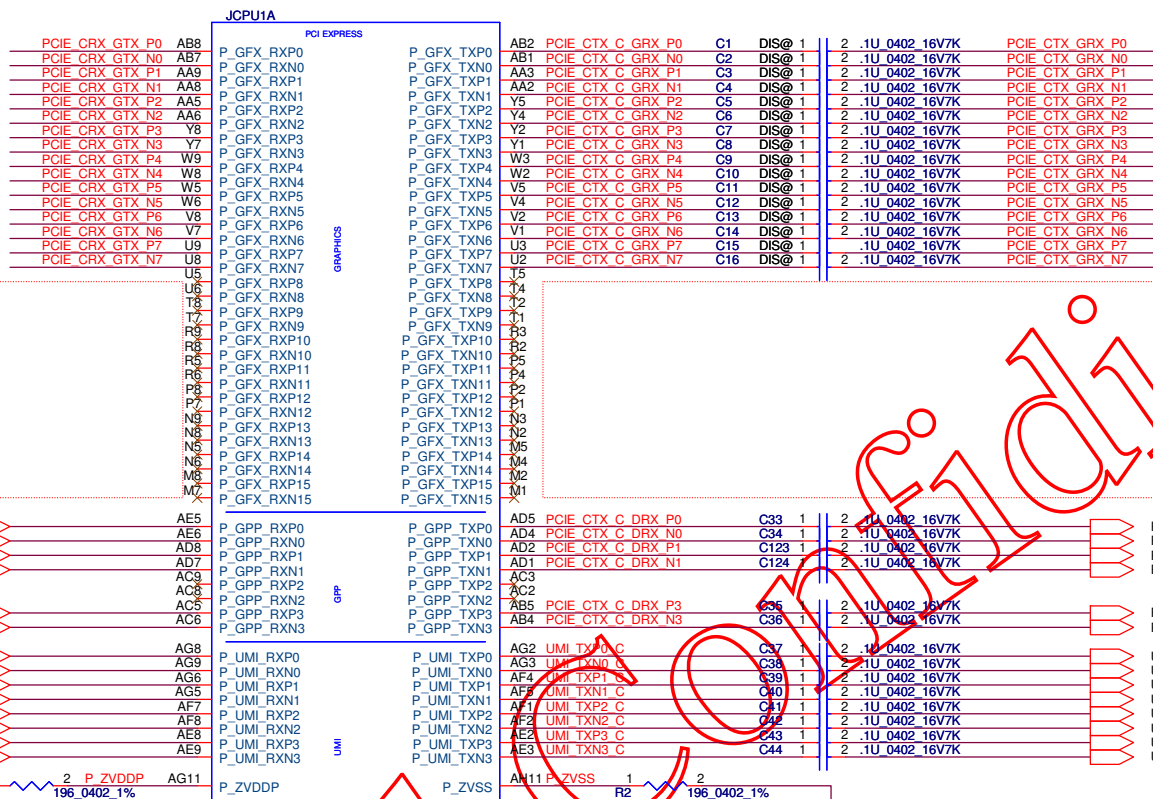
	Vendor	PS_3[2]	PS_3[1]	PS_3[0]	R_pu	R_pd
1G	H5TQ2G63DFR-11C SA00003Y070	0	0	0	R1430 NC	R1436 4.75K
	K4W2G1646E-BC11 SA00005SH00	0	0	1	R1430 8.45K	R1436 2K
	MT41J128M16JT-093G SA000067510 FBGA Code:D9PTD	0	1	0	R1430 4.53K	R1436 2K
2G	K4W4G1646B-HC11 SA000068R00	0	1	1	R1430 6.98K	R1436 4.99K
	MT41K256M16HA-107G SA000065D00 FBGA Code:D9PZD	1	0	0	R1430 4.53K	R1436 4.99K
	MT41J128M16JT-107G SA00005SM30 FBGA Code:D9PRS	1	0	1	R1430 3.24K	R1436 5.62k
1G	K4W2G1646E-BC1A SA000068U10	1	1	0	R1430 8.4k	R1436 10k
		1	1	1	R1430 4.75K	R1436 NC



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LA-8127P				Rev 1.0
Date: Tuesday, March 12, 2013				Sheet 4 of 51

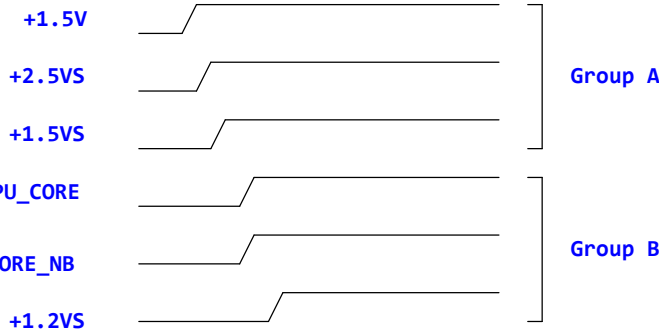
```
[17] PCIE_CRX_GTX_N[0..7]
```

> PCIE\_CTX\_GRX\_N[0..7] [17]



LAN  
WLAN

### Card Reader



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				Customer	LA-8127P
Date: Tuesday, March 12, 2013				Sheet	5 of 51

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## Place near APU

[25] DP0\_TXP0\_C  
[25] DP0\_TXN0\_C

C52 1 2 .1U 0402 16V7K DP0\_TXP0\_L3  
C47 1 2 .1U 0402 16V7K DP0\_TXN0\_L2

[13] ML\_VGA\_TXP0  
[13] ML\_VGA\_TXN0

C61 1 2 .1U 0402 16V7K DP1\_TXP0\_H5  
C62 1 2 .1U 0402 16V7K DP1\_TXN0\_H4

[13] ML\_VGA\_TXP1  
[13] ML\_VGA\_TXN1

C63 1 2 .1U 0402 16V7K DP1\_TXP1\_H2  
C64 1 2 .1U 0402 16V7K DP1\_TXN1\_H1

[13] ML\_VGA\_TXP2  
[13] ML\_VGA\_TXN2

C65 1 2 .1U 0402 16V7K DP1\_TXP2\_G3  
C66 1 2 .1U 0402 16V7K DP1\_TXN2\_G2

[13] ML\_VGA\_TXP3  
[13] ML\_VGA\_TXN3

C67 1 2 .1U 0402 16V7K DP1\_TXP3\_F2  
C68 1 2 .1U 0402 16V7K DP1\_TXN3\_F1

[27] HDMI\_TX2P  
[27] HDMI\_TX2N

C50 1 2 .1U 0402 16V7K DP2\_TXP0\_L9  
C51 1 2 .1U 0402 16V7K DP2\_TXN0\_L8

[27] HDMI\_TX1P  
[27] HDMI\_TX1N

C55 1 2 .1U 0402 16V7K DP2\_TXP1\_L5  
C56 1 2 .1U 0402 16V7K DP2\_TXN1\_L6

[27] HDMI\_TX0P  
[27] HDMI\_TX0N

C57 1 2 .1U 0402 16V7K DP2\_TXP2\_K8  
C58 1 2 .1U 0402 16V7K DP2\_TXN2\_K7

[27] HDMI\_CLKP  
[27] HDMI\_CLKN

C59 1 2 .1U 0402 16V7K DP2\_TXP3\_J6  
C60 1 2 .1U 0402 16V7K DP2\_TXN3\_J5

[12] APU\_CLK  
[12] APU\_CLK#

APU\_CLK AE11  
APU\_CLK# AD11

[12] APU\_DISP\_CLK  
[12] APU\_DISP\_CLK#

APU\_DISP\_CLK AB11  
APU\_DISP\_CLK# AA11

[45] APU\_SVC  
[45] APU\_SVD

B3  
A3

[45] APU\_SVT

C3  
SVT

[12] APU\_RST#  
[12,45] APU\_PWRGD

APU\_RST# AF10  
APU\_PWRGD AB12

[12] APU\_PROCHOT#

APU\_PROCHOT# AC10  
APU\_THERMTRIP# AE12  
APU\_ALERT# AF12

T23  
T24  
T25  
T26  
T27  
T28  
T29

APU\_TDI H10  
APU\_TDO J10  
APU\_TCK F10  
APU\_TMS G10  
APU\_TFS# F9  
APU\_DBRDY G9  
APU\_DBREQ# H9

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

Route as differential  
with VSS\_SENSE

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

[45] APU\_VDD\_SEN\_L  
[45] APU\_VDDNB\_SEN

APU\_VDD\_SEN\_L B4  
APU\_VDDNB\_SEN A4

[45] APU\_VDD\_SEN\_H

APU\_VDD\_SEN\_H B5  
APU\_ALERT# AF12

## JCPU10

## ANALOG/DISPLAY/MISC

## LVDS

## DISPLAY PORT 0

## DISPLAY PORT 1

## DISPLAY PORT 2

## TEST

## SERIAL

## CTRL

## JTAG

## SENSE

## JCPU10

## ANALOG/DISPLAY/MISC

## LVDS

## DISPLAY PORT 0

## DISPLAY PORT 1

## DISPLAY PORT 2

## TEST

## SERIAL

## CTRL

## JTAG

## SENSE

## JCPU10

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## SENSE

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## JTAG

## SENSE

## JCPU10

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## DISPLAY PORT 1

## DISPLAY PORT 2

## TEST

## SERIAL

## CTRL

## JTAG

## SENSE

## JCPU10

## ANALOG/DISPLAY/MISC

## LVDS

## DISPLAY PORT 0

## DISPLAY PORT 1

## DISPLAY PORT 2

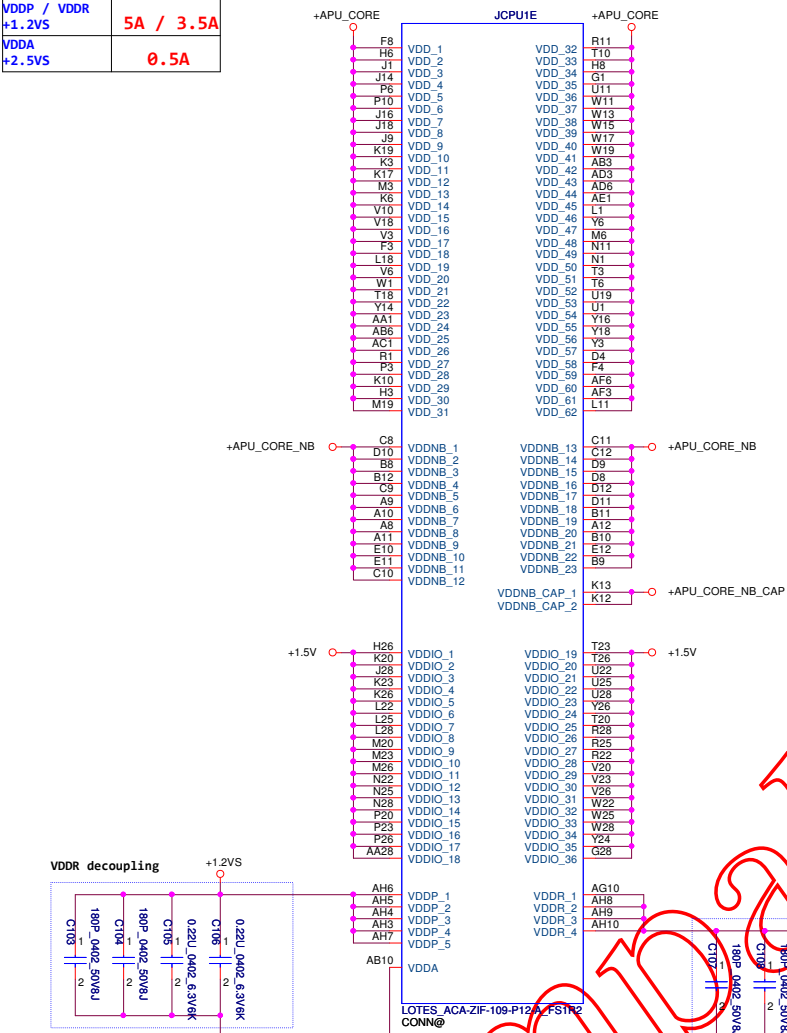
## TEST

## SERIAL

## CTRL

## JTAG

Power Name	Consumption
VDD	
+APU_CORE	60A
VDDNB	
+APU_CORE_NB	44A
VDDIO	
+1.5V	3.2A
VDDP / VDDR	
+1.2VS	5A / 3.5A
VDDA	
+2.5VS	0.5A

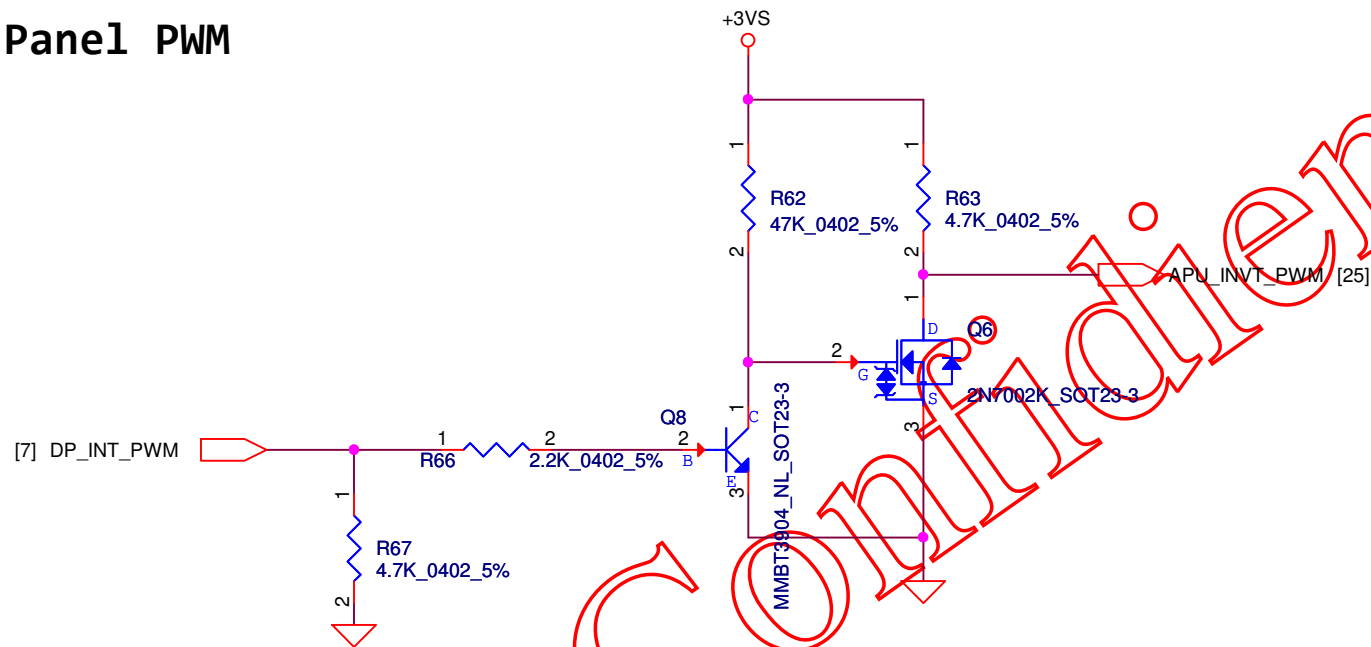


J20	JCPU1F	A19
L4	VSS_1	VSS_73
R7	VSS_2	VSS_74
W18	VSS_3	VSS_75
A15	VSS_4	VSS_76
AB17	VSS_5	VSS_77
AC22	VSS_6	VSS_78
AF24	VSS_7	VSS_79
AH23	VSS_8	VSS_80
AH25	VSS_9	VSS_81
B7	VSS_10	VSS_82
C14	VSS_11	VSS_83
C16	VSS_12	VSS_84
C2	VSS_13	VSS_85
C22	VSS_14	VSS_86
C25	VSS_15	VSS_87
C28	VSS_16	VSS_88
D13	VSS_17	VSS_89
D15	VSS_18	VSS_90
D17	VSS_19	VSS_91
D27	VSS_20	VSS_92
E4	VSS_21	VSS_93
E9	VSS_22	VSS_94
F14	VSS_23	VSS_95
F16	VSS_24	VSS_96
F18	VSS_25	VSS_97
F20	VSS_26	VSS_98
F22	VSS_27	VSS_99
F24	VSS_28	VSS_100
F26	VSS_29	VSS_101
F28	VSS_30	VSS_102
F30	VSS_31	VSS_103
F32	VSS_32	VSS_104
F34	VSS_33	VSS_105
F36	VSS_34	VSS_106
F38	VSS_35	VSS_107
F40	VSS_36	VSS_108
F42	VSS_37	VSS_109
F44	VSS_38	VSS_110
F46	VSS_39	VSS_111
F48	VSS_40	VSS_112
F50	VSS_41	VSS_113
F52	VSS_42	VSS_114
F54	VSS_43	VSS_115
F56	VSS_44	VSS_116
F58	VSS_45	VSS_117
F60	VSS_46	VSS_118
F62	VSS_47	VSS_119
F64	VSS_48	VSS_120
F66	VSS_49	VSS_121
F68	VSS_50	VSS_122
F70	VSS_51	VSS_123
F72	VSS_52	VSS_124
F74	VSS_53	VSS_125
F76	VSS_54	VSS_126
F78	VSS_55	VSS_127
F80	VSS_56	VSS_128
F82	VSS_57	VSS_129
F84	VSS_58	VSS_130
F86	VSS_59	VSS_131
F88	VSS_60	VSS_132
F90	VSS_61	VSS_133
F92	VSS_62	VSS_134
F94	VSS_63	VSS_135
F96	VSS_64	VSS_136
F98	VSS_65	VSS_137
F100	VSS_66	VSS_138
F102	VSS_67	VSS_139
F104	VSS_68	VSS_140
F106	VSS_69	VSS_141
F108	VSS_70	VSS_142
F110	VSS_71	VSS_143
F112	VSS_72	VSS_144

Demo Board Capacitor			
APU_CORE	CORE_NB	CORE_NB_CAP	VDDIO_SUS
22uF x 10	22uF x 2	22uF x 2	(CPU side)
0.22uF x 2	10uF x 1	180pF x 1	22uF x 4
0.01uF x 3	0.22uF x 2		4.7uF x 4
180pF x 2	180pF x 3		0.22uF x 6 +2(split)
			180pF x 1 + 2(split)
VDDP	VDDR	VDDA	VDDIO_SUS
0.22uF x 2	0.22uF x 2	4.7uF x 1	(DIMM x2)
180pF x 2	1nF x 4	0.22uF x 1	100uF x 2
	180pF x 2	3.3nF x 1	0.1uF x 12

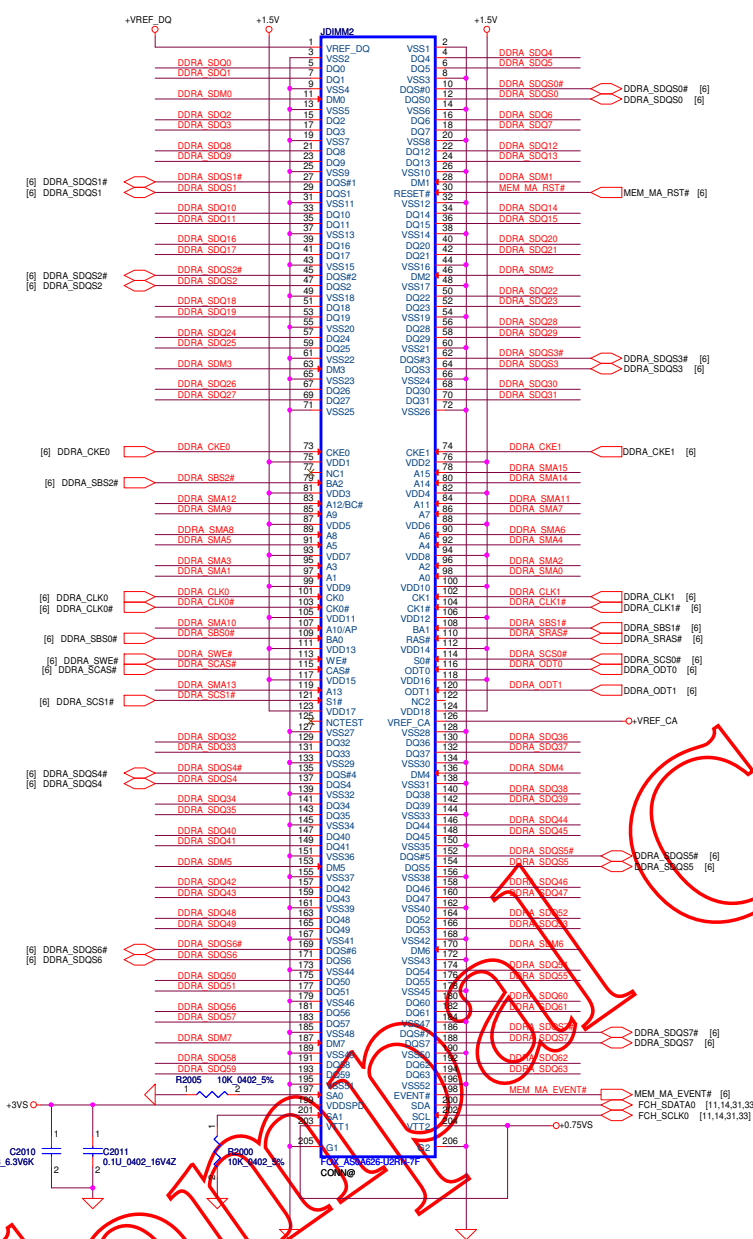


# Panel PWM

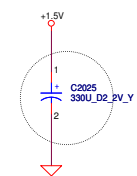
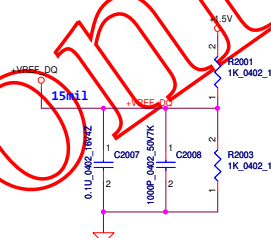
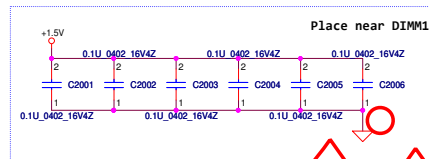
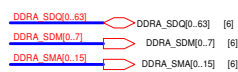


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Date: Tuesday, March 12, 2013				Sheet	9 of 51
Rev				1.0	

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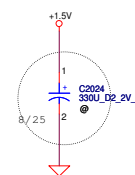
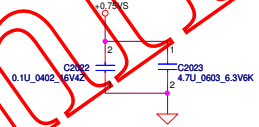
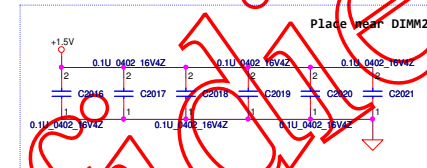
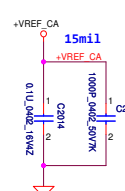
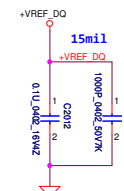


Reverse H:5.2mm

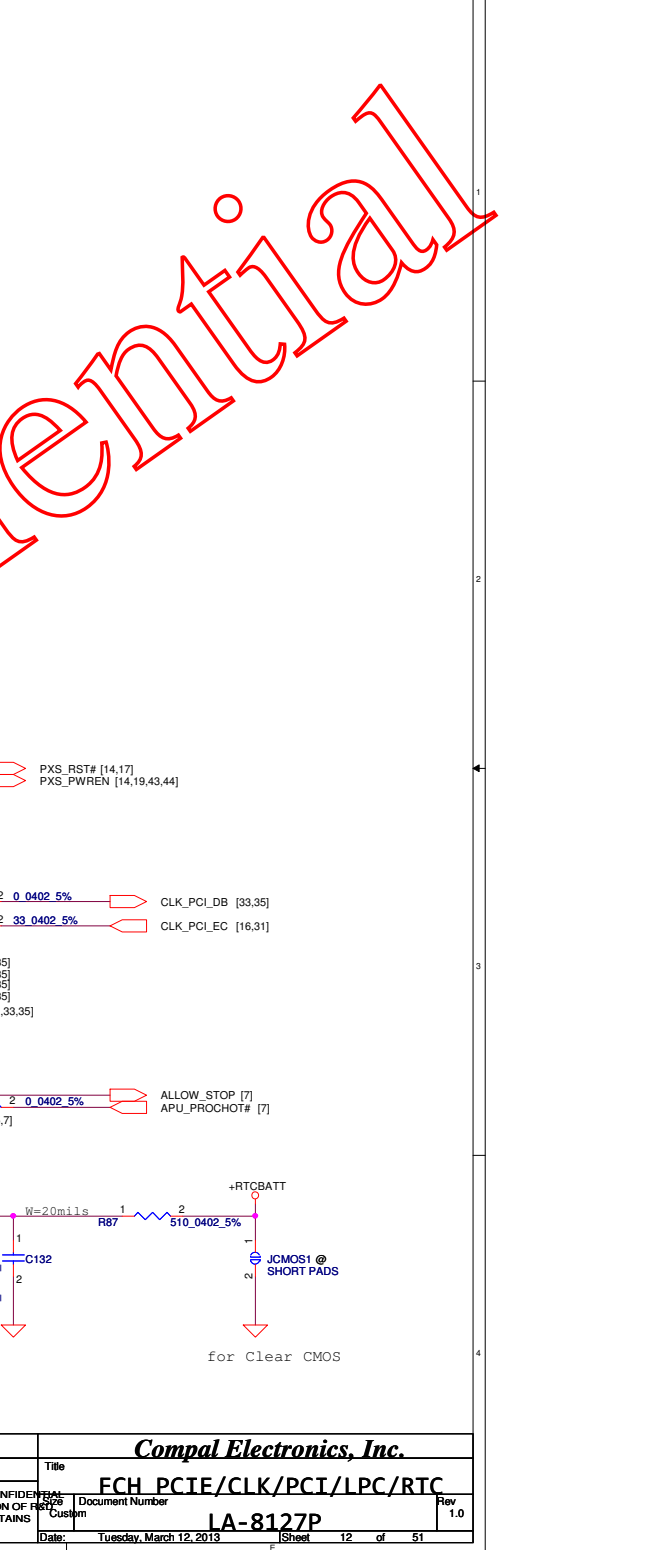
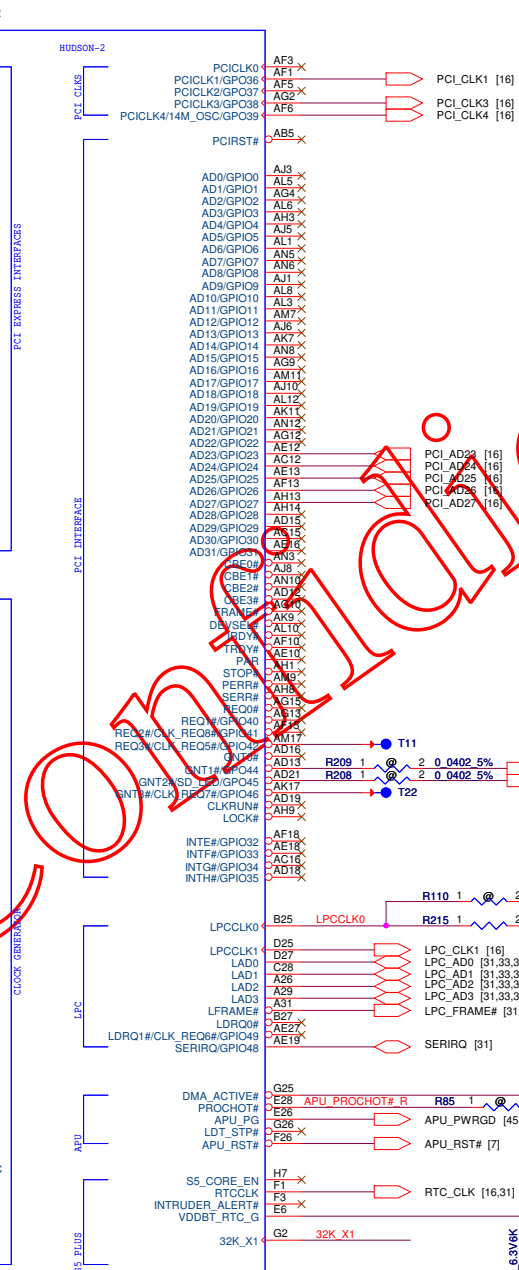


Reverse H:9.2mm

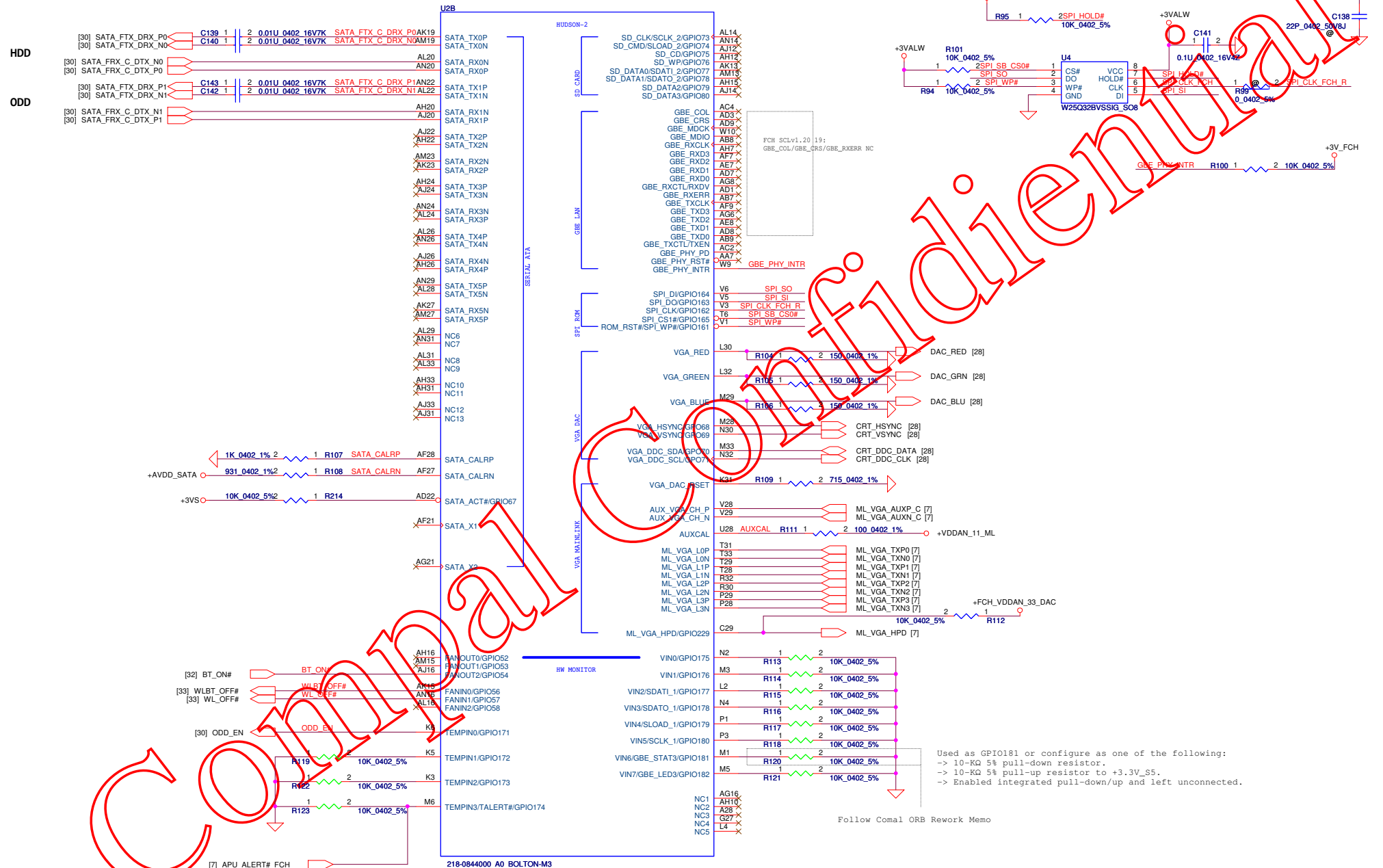
DDR8\_SDO[0..63] DDR8\_SDO[0..63] [6]  
DDR8\_SDM[0..7] DDR8\_SDM[0..7] [6]  
DDR8\_SMA[0..15] DDR8\_SMA[0..15] [6]



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Size	C	Document Number	LA-8127P	Rev 1.0
Date:	Tuesday, March 12, 2013	Sheet	11	of 51



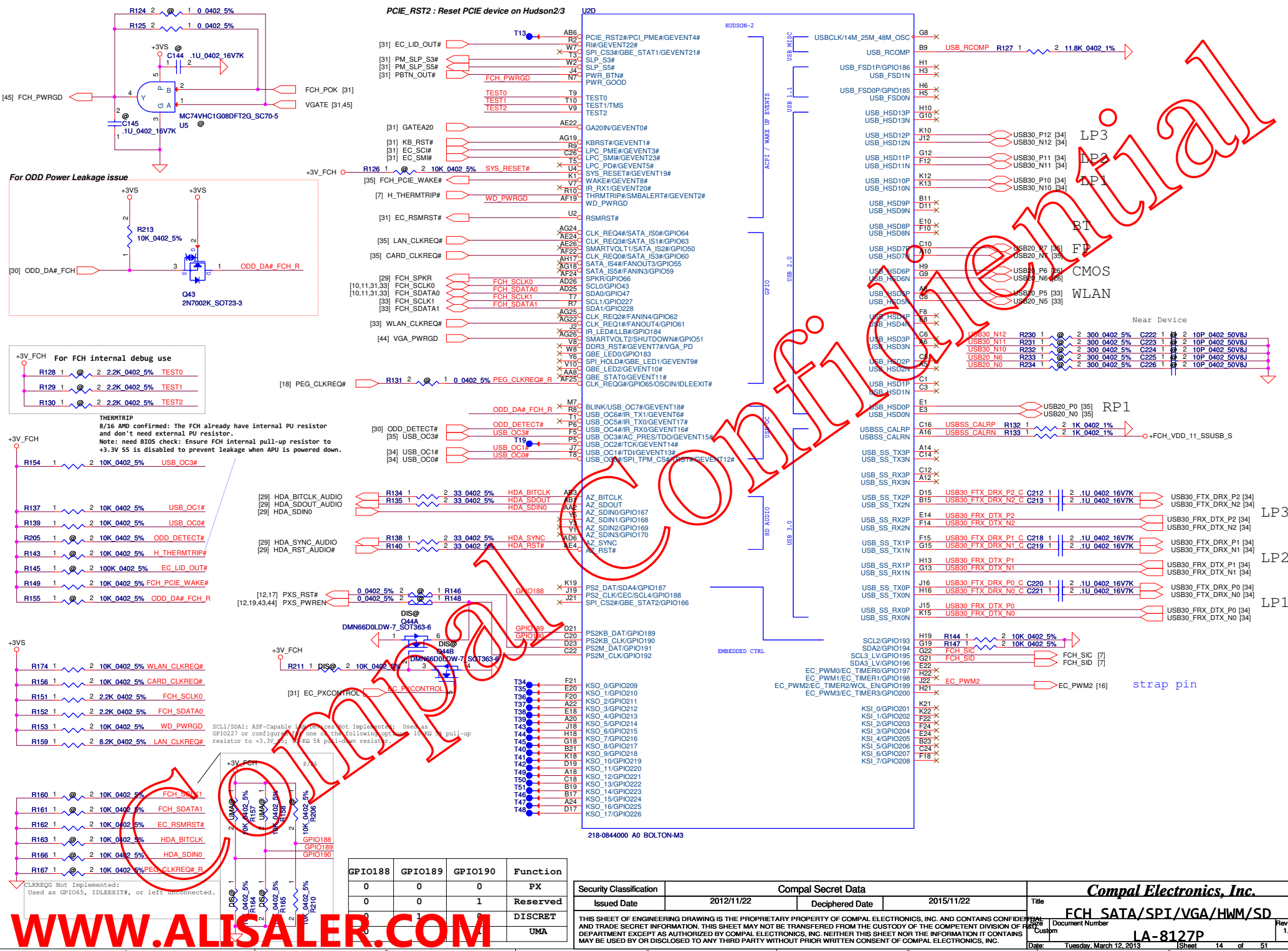
**4MB SPI ROM  
& Non-share ROM.**



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Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> <b>FCH SATA/SPT/VGA/HWM/SD</b>	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	FCH SATA/SPT/VGA/HWM/SD Document Number <b>LA-8127P</b>
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Issued Date	2012/11/22	Deciphered Date	2015/11/22	FCH SATA/SPI/VGA/HWM/SD	
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Date		Tuesday, March 12, 2013		LA-8127P	
		Sheet		14 of 51	





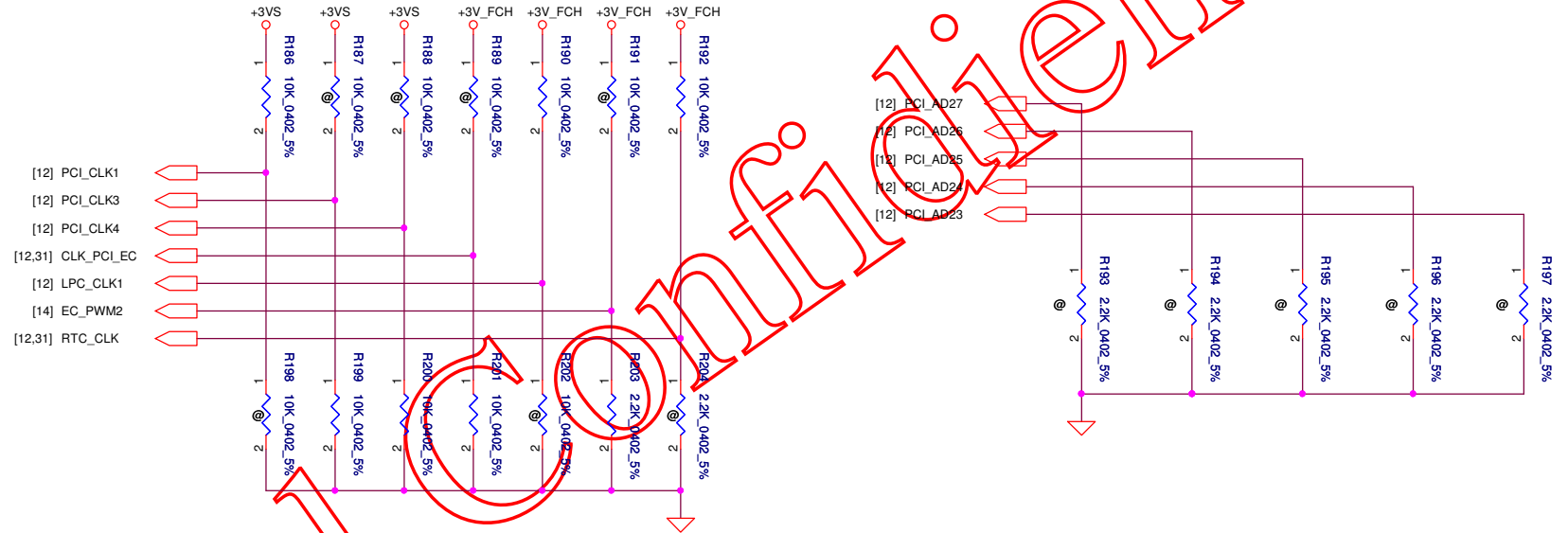
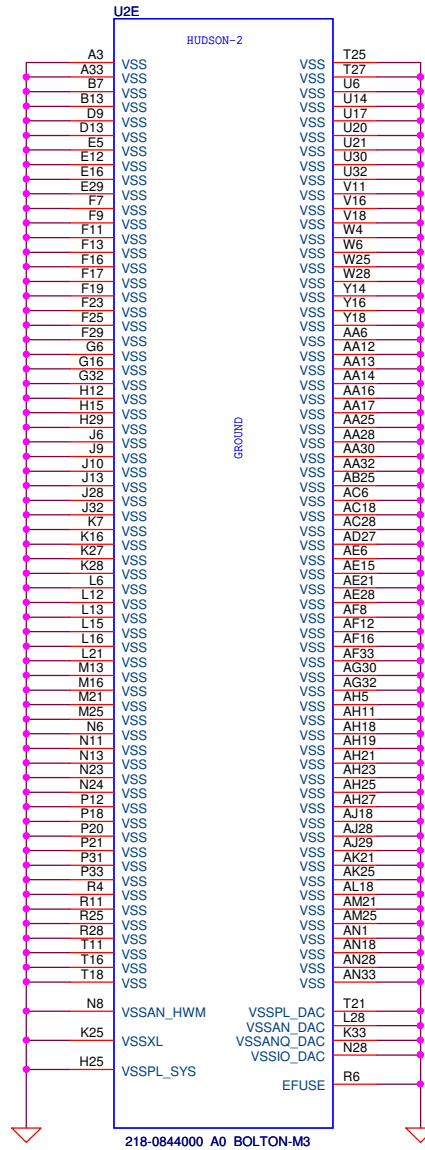
## STRAP PINS

	PCI_CLK1	PCI_CLK3	PCI_CLK4	CLK_PCI_EC	LPC_CLK1	EC_PWM2	RTC_CLK
<b>PULL HIGH</b>	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
<b>PULL LOW</b>	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED

## DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI\_AD[27:23]

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
<b>PULL LOW</b>	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



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				LA-8127P
				Rev 1.0
				Date: Tuesday, March 12, 2013
				Sheet 16 of 51

[5] PCIE\_CTX\_GRX\_P[7..0] → PCIE\_CTX\_GRX\_P[7..0]  
[5] PCIE\_CTX\_GRX\_N[7..0] → PCIE\_CTX\_GRX\_N[7..0]

SDV/FVT, NO.3  
U1401A

PCIE\_TX0P  
PCIE\_TX0N

PCIE\_CTX\_GRX\_P0 AA38  
PCIE\_CTX\_GRX\_N0 Y37

PCIE\_CTX\_GRX\_P1 Y35  
PCIE\_CTX\_GRX\_N1 W36

PCIE\_CTX\_GRX\_P2 W38  
PCIE\_CTX\_GRX\_N2 V37

PCIE\_CTX\_GRX\_P3 V35  
PCIE\_CTX\_GRX\_N3 U36

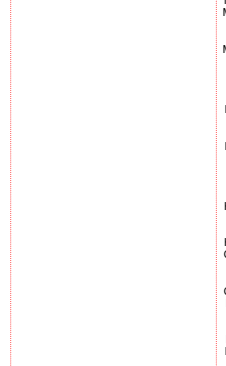
PCIE\_CTX\_GRX\_P4 U38  
PCIE\_CTX\_GRX\_N4 T37

PCIE\_CTX\_GRX\_P5 T35  
PCIE\_CTX\_GRX\_N5 R36

PCIE\_CTX\_GRX\_P6 R38  
PCIE\_CTX\_GRX\_N6 P37

PCIE\_CTX\_GRX\_P7 P35  
PCIE\_CTX\_GRX\_N7 N36

SDV/FVT, NO.1



PCI EXPRESS INTERFACE

PCIE\_CRX\_GTX\_P[7..0] → PCIE\_CRX\_GTX\_P[7..0] [5]  
PCIE\_CRX\_GTX\_N[7..0] → PCIE\_CRX\_GTX\_N[7..0] [5]

PCIE\_TX0P  
PCIE\_TX0N

Y33 PCIE\_CRX\_C GTX\_P0 .1U 0402 16V7K 2  
Y32 PCIE\_CRX\_C GTX\_N0 .1U 0402 16V7K 2

PCIE\_TX1P  
PCIE\_TX1N

W33 PCIE\_CRX\_C GTX\_P1 .1U 0402 16V7K 2  
W32 PCIE\_CRX\_C GTX\_N1 .1U 0402 16V7K 2

PCIE\_TX2P  
PCIE\_TX2N

U33 PCIE\_CRX\_C GTX\_P2 .1U 0402 16V7K 2  
U32 PCIE\_CRX\_C GTX\_N2 .1U 0402 16V7K 2

PCIE\_TX3P  
PCIE\_TX3N

U30 PCIE\_CRX\_C GTX\_P3 .1U 0402 16V7K 2  
U29 PCIE\_CRX\_C GTX\_N3 .1U 0402 16V7K 2

PCIE\_TX4P  
PCIE\_TX4N

T33 PCIE\_CRX\_C GTX\_P4 .1U 0402 16V7K 2  
T32 PCIE\_CRX\_C GTX\_N4 .1U 0402 16V7K 2

PCIE\_TX5P  
PCIE\_TX5N

T30 PCIE\_CRX\_C GTX\_P5 .1U 0402 16V7K 2  
T29 PCIE\_CRX\_C GTX\_N5 .1U 0402 16V7K 2

PCIE\_TX6P  
PCIE\_TX6N

P33 PCIE\_CRX\_C GTX\_P6 .1U 0402 16V7K 2  
P32 PCIE\_CRX\_C GTX\_N6 .1U 0402 16V7K 2

PCIE\_TX7P  
PCIE\_TX7N

P30 PCIE\_CRX\_C GTX\_P7 .1U 0402 16V7K 2  
P29 PCIE\_CRX\_C GTX\_N7 .1U 0402 16V7K 2

SDV/FVT, NO.2



[12] CLK\_PCIE\_VGA  
[12] CLK\_PCIE\_VGA#

CLK\_PCIE\_VGA AB35  
CLK\_PCIE\_VGA# AA36

CLOCK

PCIE\_REFCLKP  
PCIE\_REFCLKN

TEST\_PG AH16  
GPU\_RST# AA30

PERST# AA30

CALIBRATION

PCIE\_CALR\_TX  
PCIE\_CALR\_RX

Y30 R1404 1 DIS@ 2 1.69K 0402 1% 0.95VGS  
Y29 R1405 1 DIS@ 2 1K 0402 1% 0.95VGS

## LVDS Interface

U1401D

RSVD/VARY BL  
RSVD/DIGON

TXCBP\_DPB3P  
TXCBM\_DPB3N

TX3M\_DPB2N  
TX3M\_DPB2P

TX4P\_DPB1P  
TX4M\_DPB1N

TX5P\_DPB0P  
TX5M\_DPB0N

NC#AF35  
NC#AG36

TXCAP\_DPA3P  
TXCAM\_DPA3N

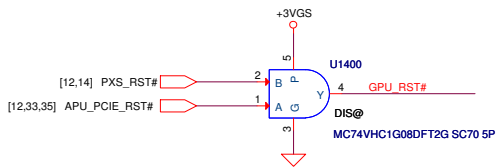
TX0P\_DPA2P  
TX0M\_DPA2N

TX1P\_DPA1P  
TX1M\_DPA1N

TX2P\_DPA0P  
TX2M\_DPA0N

NC  
NC

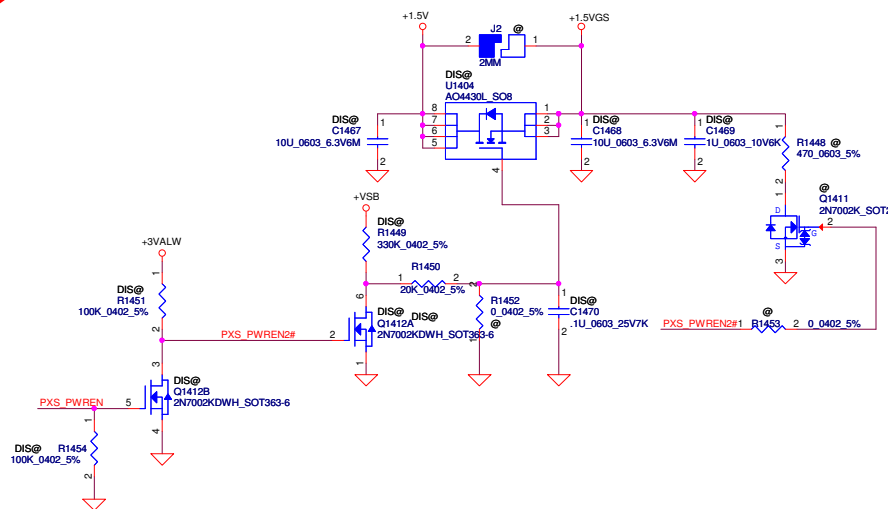
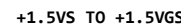
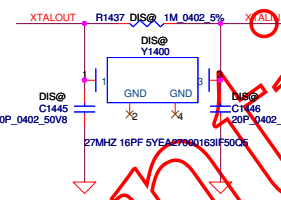
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				Date	Tuesday, March 12, 2013	Sheet 17 of 51

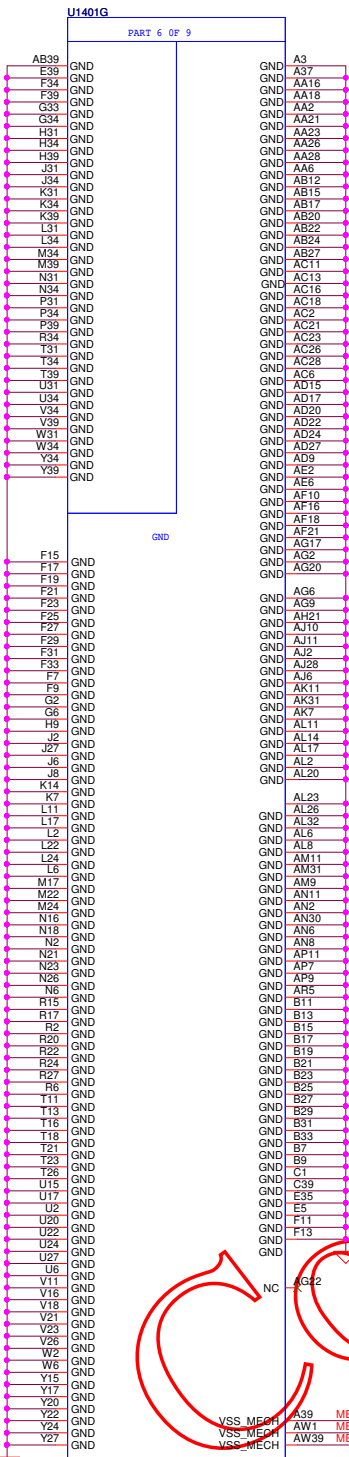


SPLL_VDDC	MarsCRB	Design
120ohm	1	1
0.1u	1	1
1u	1	1
10u	1	1



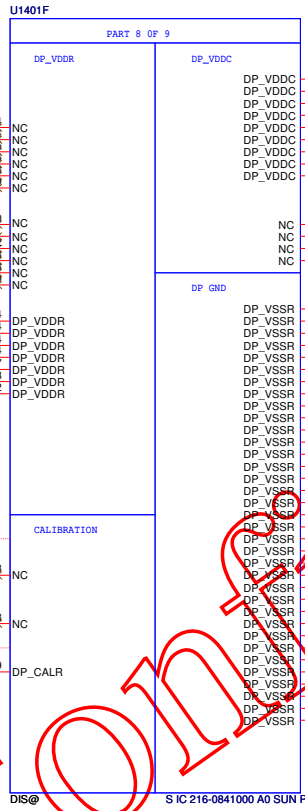
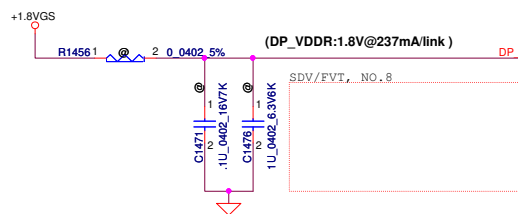
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				Customer	1.0
				Date:	Tuesday, March 12, 2013
				Sheet	19 of 51



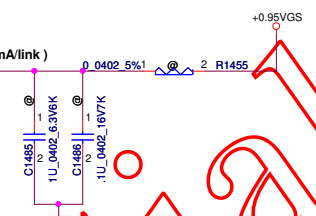


DP_VDDR	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

AMD:  
no display from GPU,  
can uninstall the capacitors



(DP\_VDDC:0.95V@280mA/link)

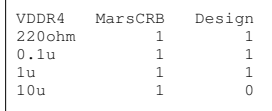


DP_VDDC	MarsCRB	Design
0.1u	1	1
1u	1	1
10u	1	1

DIS@ S IC 216-0841000 A0 SUN PRO M2 FCBGA 962P A39



(VDDR1:1.5V@3A,GDDR5:1125MHz )



for Sun Pro Ball name AD12,AF11,AF12,AF13,AF15,AG11,AG13,AG15 is NC

Route as differential pair



AG28

FB\_

AH29 ER (

10-3	
------	--

100

100

7

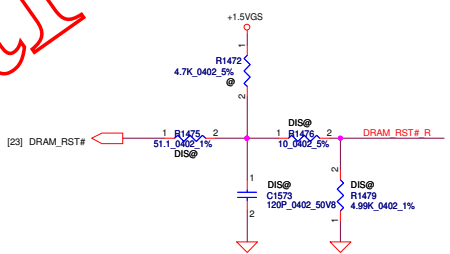
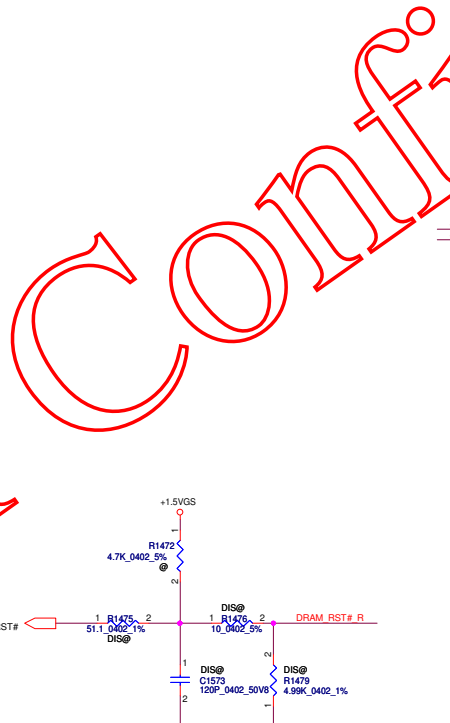
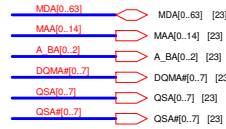
DISC

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S IC 216-0841000 A0 SUN PRO M2 FCBGA 962P A39

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				Size C	Document Number	Rev 1.0
				LA-8127P		
Date: Tuesday, March 12, 2013		Sheet 21 of 51				

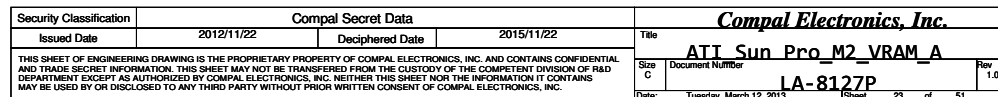
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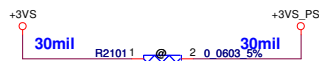
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Issued Date		2012/11/22		Deciphered Date		2015/11/22	
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				ATI Sun Pro M2 MEM IF			
				Size	Document Number		Rev
					LA-8127P		1.0
				Date:	Tuesday, March 12, 2013		Sheet 22 of 51

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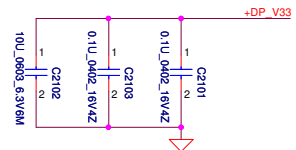


Compal Confidential

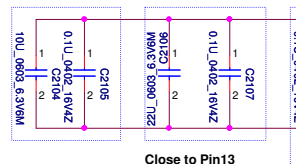
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Issued Date		Deciphered Date		2015/11/22	
2012/11/22		2015/11/22		ATT Sun Pro M2 VRAM B	
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		C		LA-8127P	1.0
Date:		Tuesday, March 12, 2013		Sheet	24 of 51



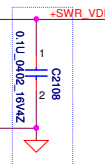
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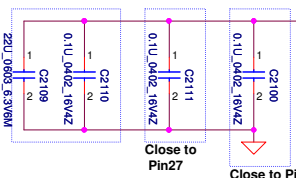
Close to L27



Close to Pin18

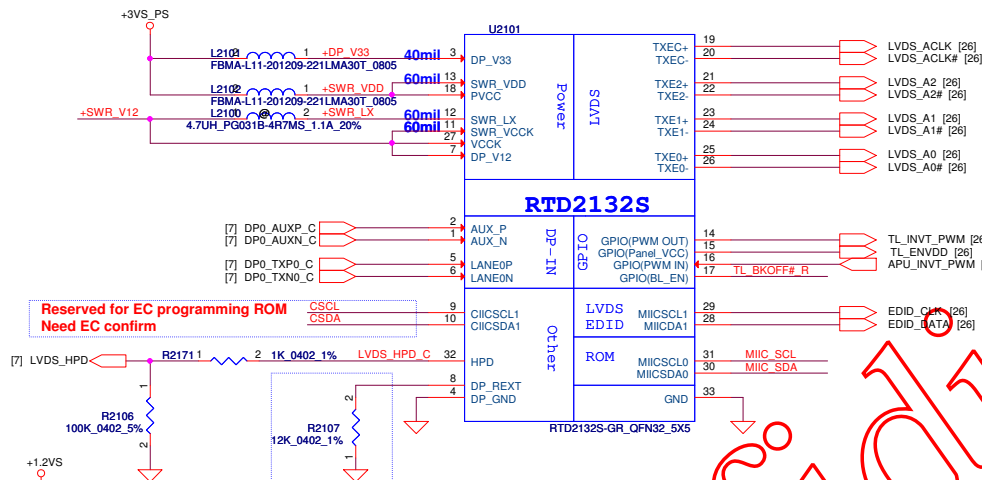


Close to L29



Compal

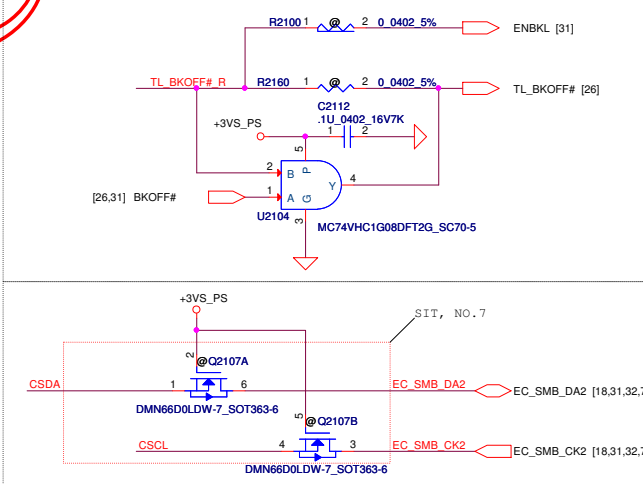
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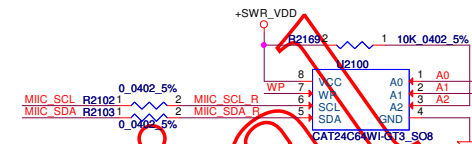
Reserved for EC programming ROM  
Need EC confirm

Change to 12Kohm 1% (DG ref.)  
20101114

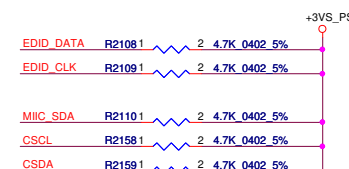
Vendor advise reserve it



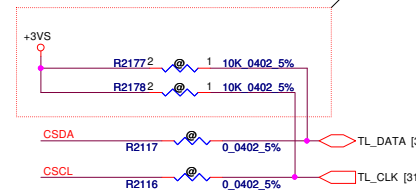
EEROM



2132S-Ver E: External ROM, pin31 PU +3VS  
Internal RAM support, pin31 PD to GND  
EEROM EEROM EEROM EEROM



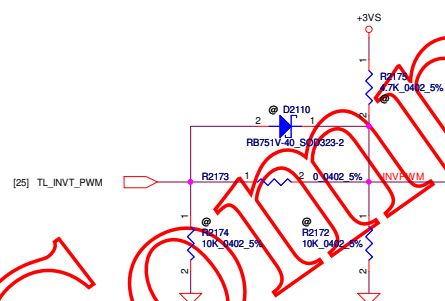
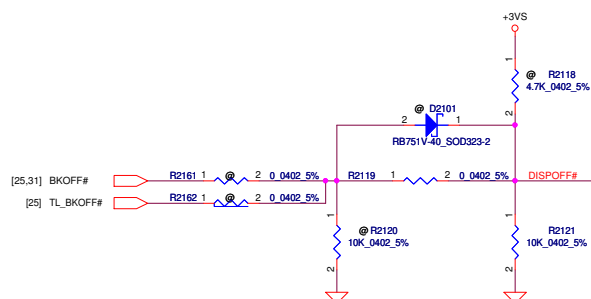
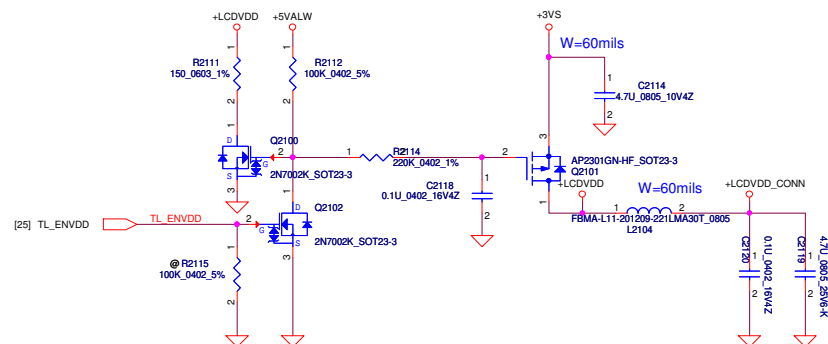
Vendor Suggest 2011.08.15



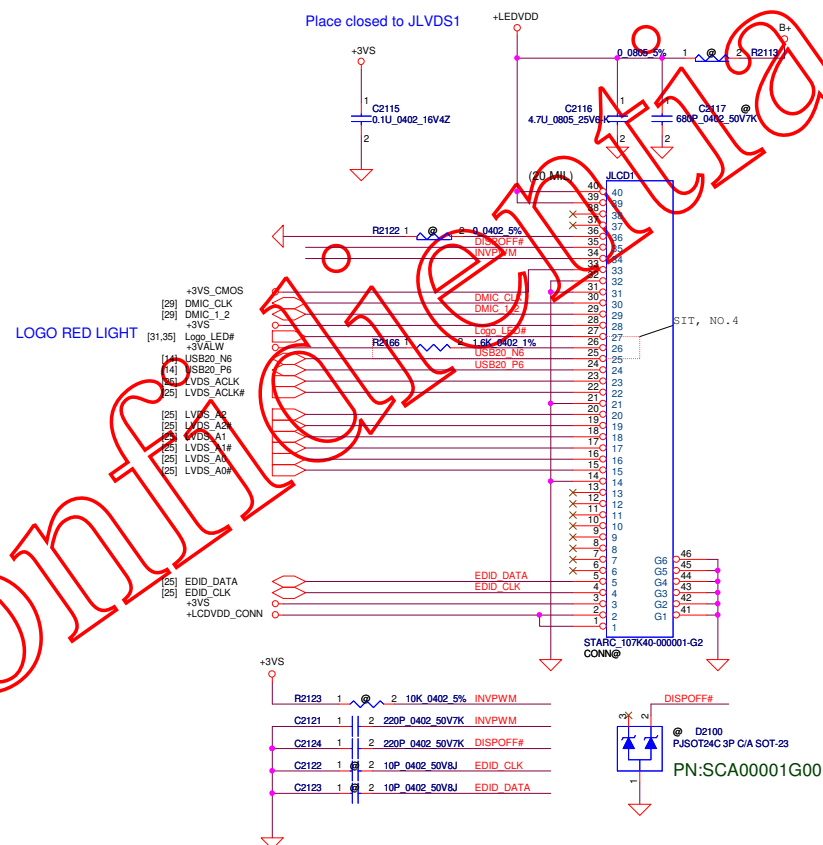
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Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title
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				LA-8127P
				Rev 1.0
				Date: Tuesday, March 12, 2013
				Sheet 25 of 51

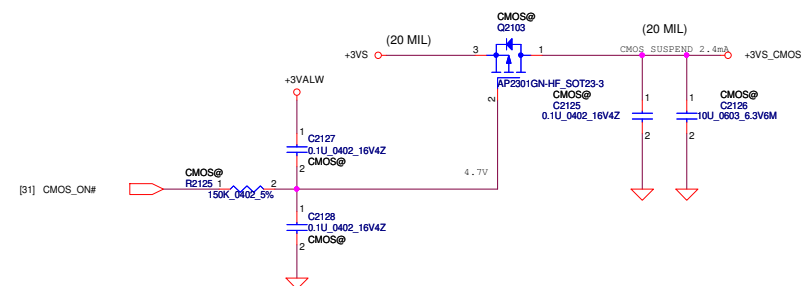
## LCD POWER CIRCUIT



**LCD/LED PANEL Conn.**



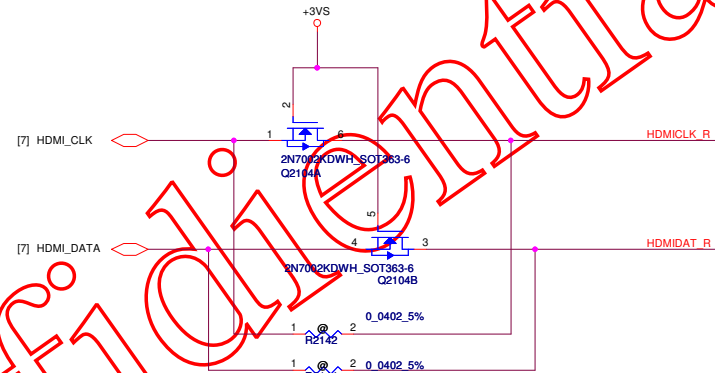
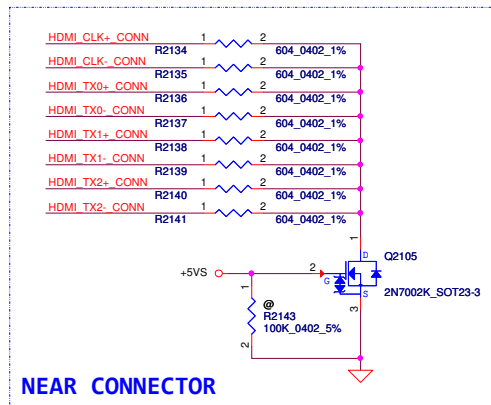
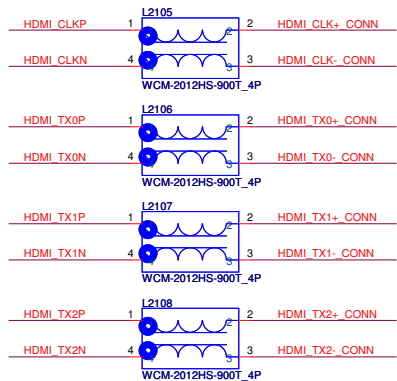
## CMOS Camera Conn



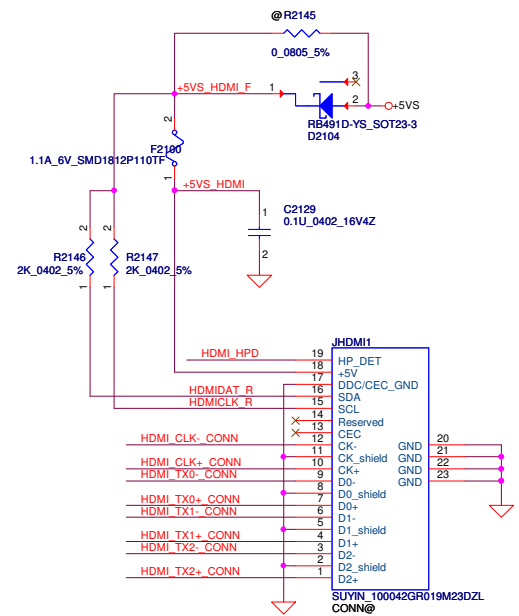
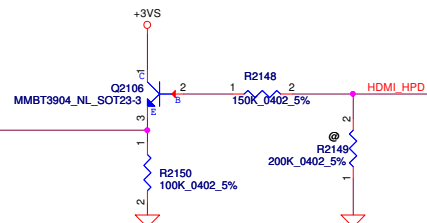
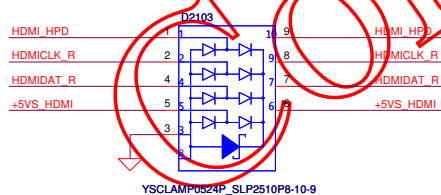
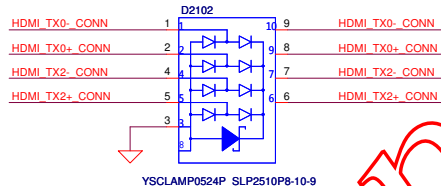
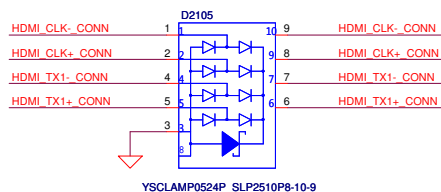
Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i>				
Issued Date		2012/11/22	Deciphered Date		2015/11/22	Title		
						LVDS CONN/CAMERA		
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						Custn	LA-8127P	
						Date:	Tuesday, March 12, 2013	Sheet 26 of 51



[7] HDMI_CLKP	R2126	1	2	0	0402_5%	HDMI_CLK+ CONN
[7] HDMI_CLKN	R2127	1	2	0	0402_5%	HDMI_CLK- CONN
[7] HDMI_TX0P	R2128	1	2	0	0402_5%	HDMI_TX0+ CONN
[7] HDMI_TX0N	R2129	1	2	0	0402_5%	HDMI_TX0- CONN
[7] HDMI_TX1P	R2130	1	2	0	0402_5%	HDMI_TX1+ CONN
[7] HDMI_TX1N	R2131	1	2	0	0402_5%	HDMI_TX1- CONN
[7] HDMI_TX2P	R2132	1	2	0	0402_5%	HDMI_TX2+ CONN
[7] HDMI_TX2N	R2133	1	2	0	0402_5%	HDMI_TX2- CONN

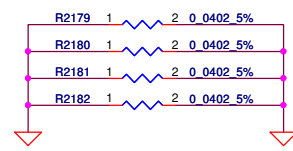
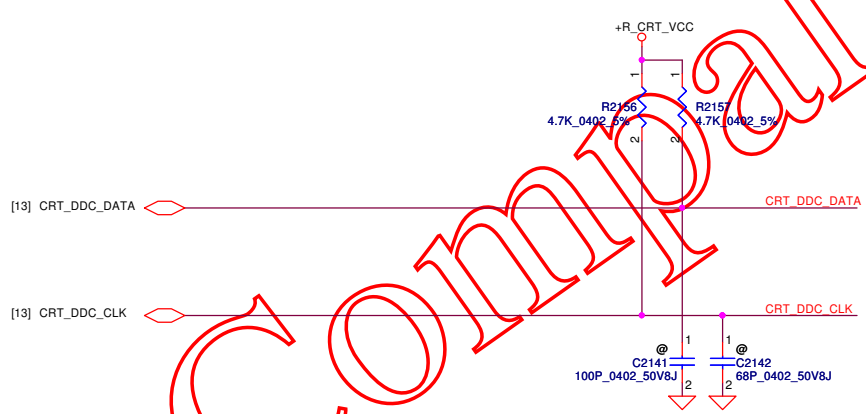
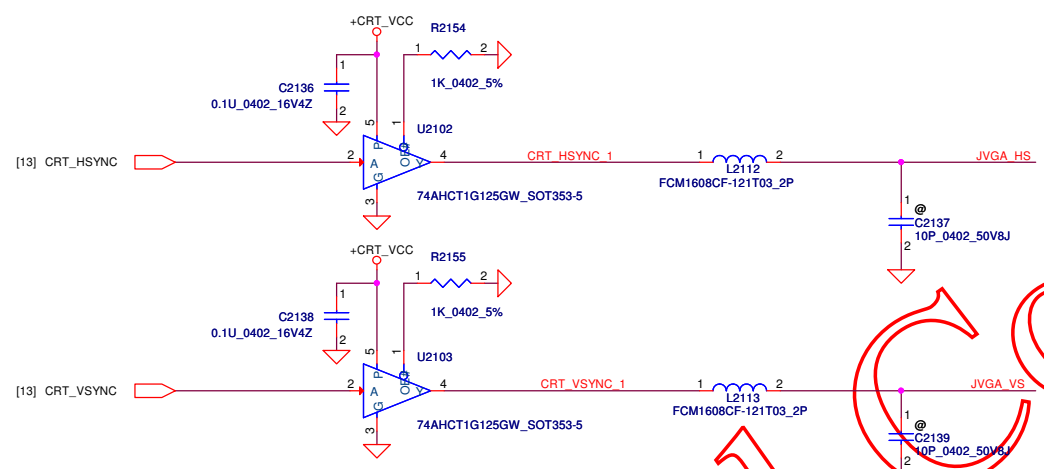
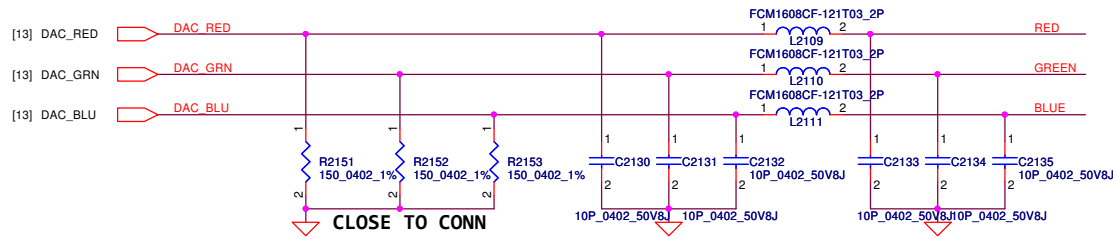


## ESD Request

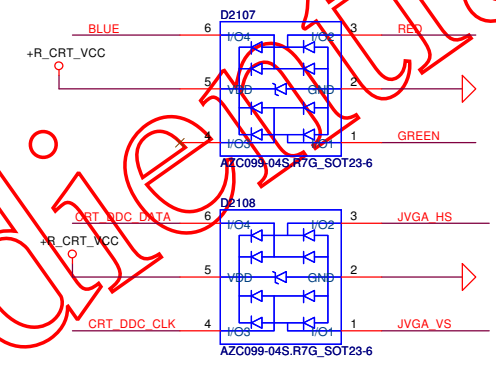


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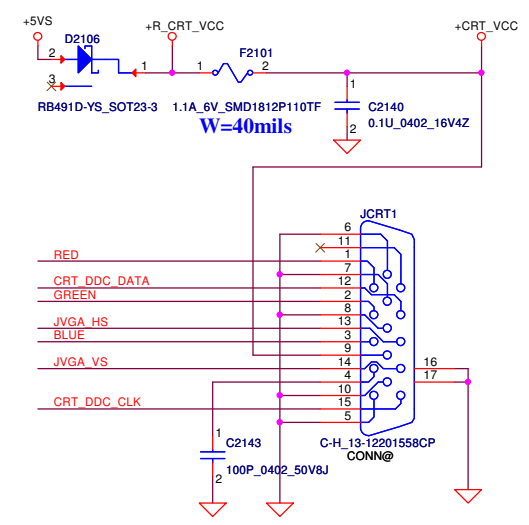
Security Classification	Compal Secret Data		Title	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	HDMI Connector
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Date: Tuesday, March 12, 2013				Sheet 27 of 51



## ESD Request



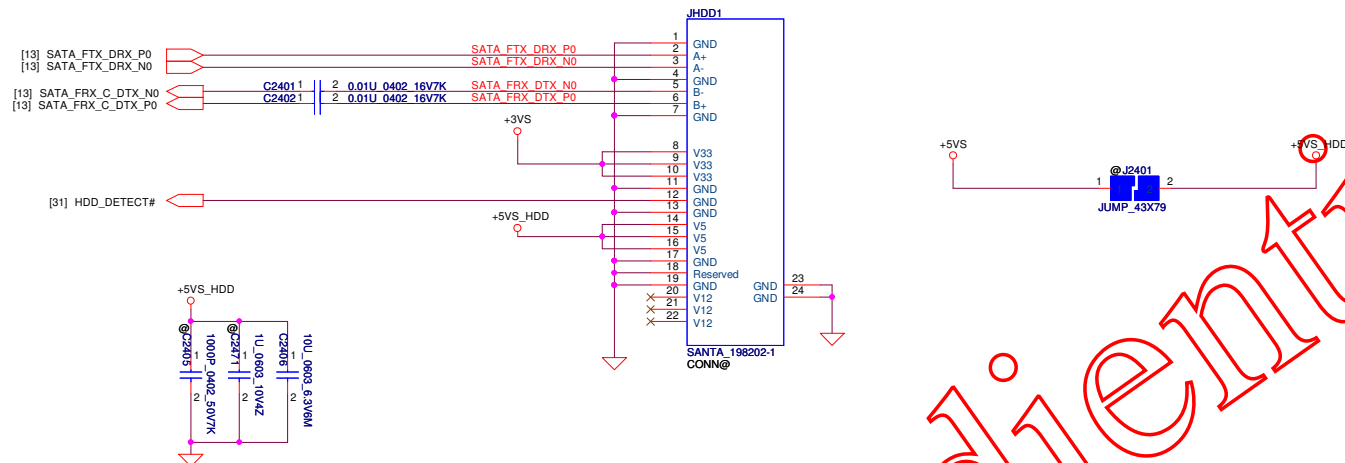
## CRT Connector



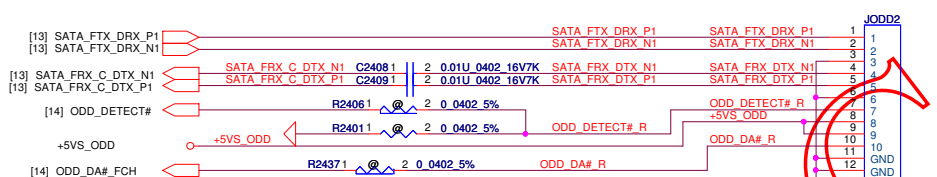
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	
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Size	Custom	Document Number	LA-8127P	Rev 1.0	
Date:	Tuesday, March 12, 2013	Sheet	28	of 51	



**SATA HDD Conn.**



**SATA ODD Conn.**

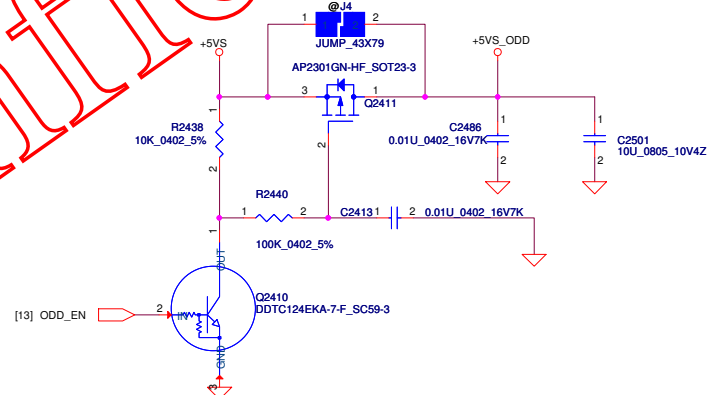


Note.

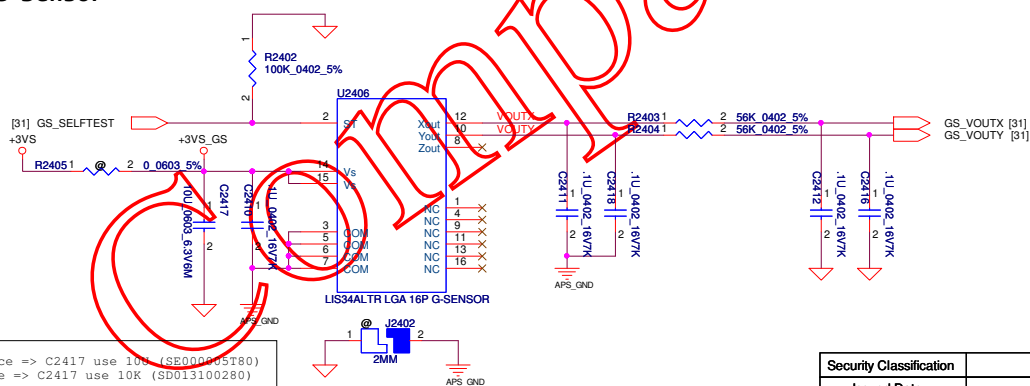
QALEA 14" => JODD1

QALEB 15" => JODD2

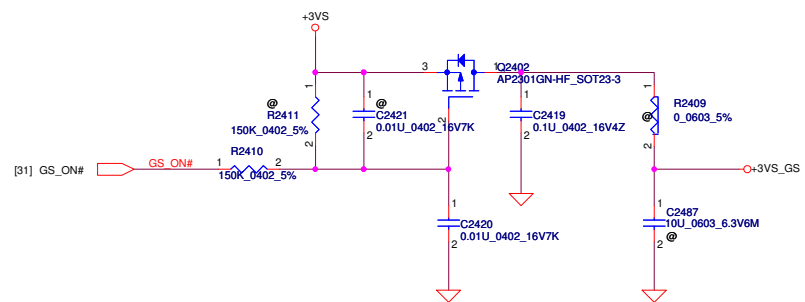
~~ODD~~ Power Control



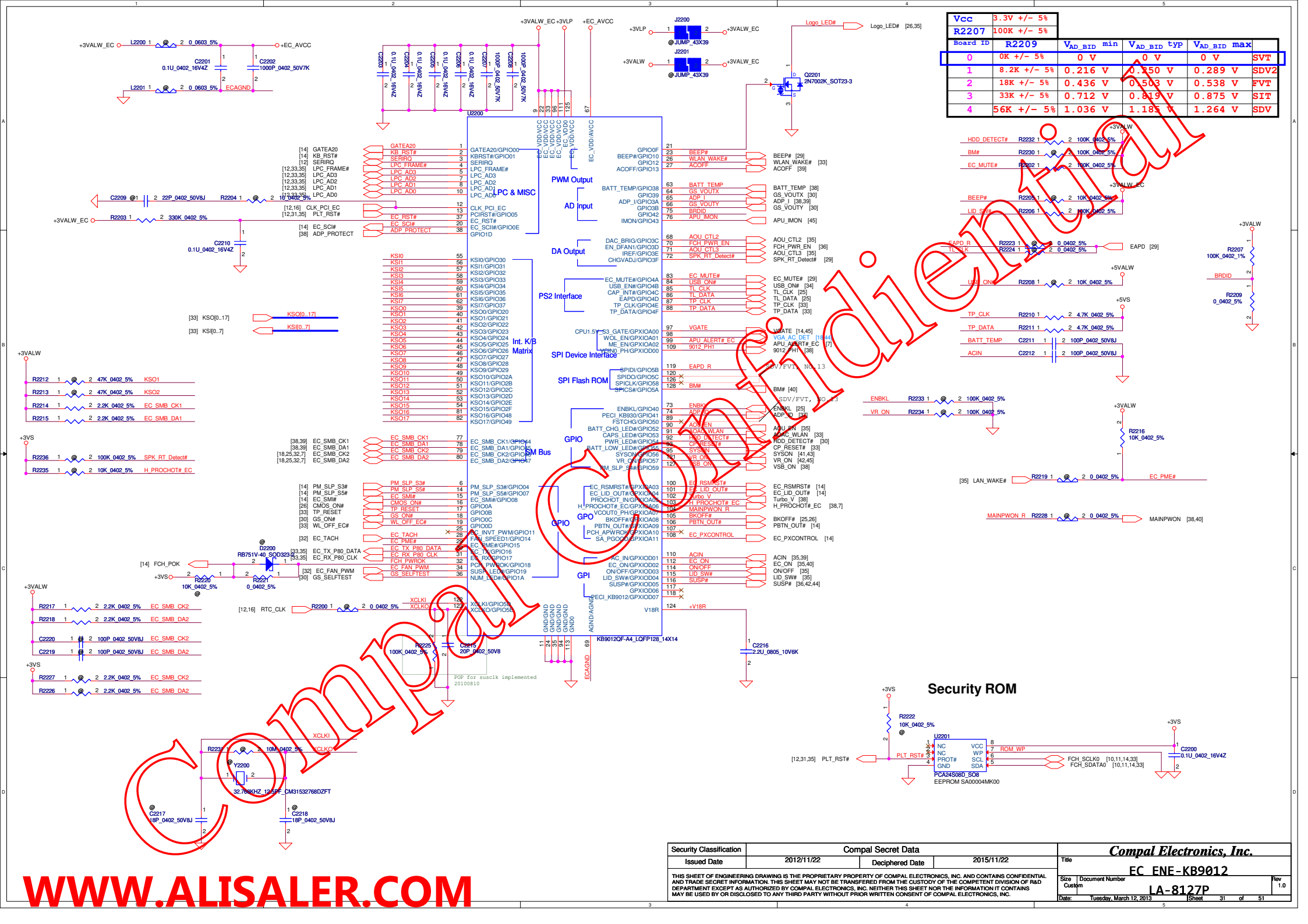
## APS G-Sensor



Note.  
Main Source => C2417 use 100 (SE000005T80)  
2nd Source => C2417 use 10K (SD013100280)



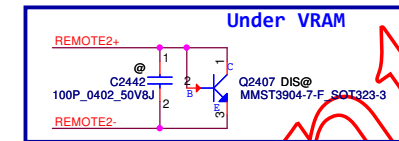
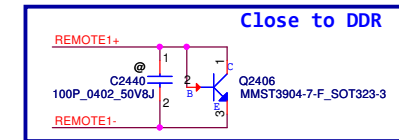
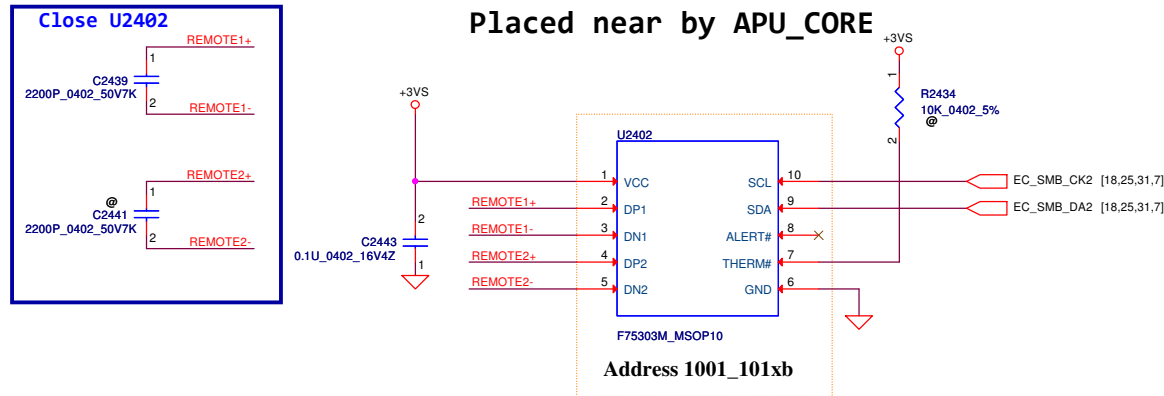
Security Classification		Compal Secret Data		<b>Compal Electronics, Inc.</b> Title: <b>HDD/ODD/G-Sensor</b>	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Document Number	<b>LA-8127P</b> Date: Tuesday, March 12, 2013 Sheet 30 of 51
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Vcc	3.3V +/- 5%				
R2207	100K +/- 5%				
Board ID	R2209	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	
0	0K +/- 5%	0 V	0 V	0 V	SVT
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V	SDV2
2	18K +/- 5%	0.436 V	0.503 V	0.538 V	FVT
3	33K +/- 5%	0.712 V	0.819 V	0.875 V	STT
4	56K +/- 5%	1.036 V	1.185 V	1.264 V	SDV

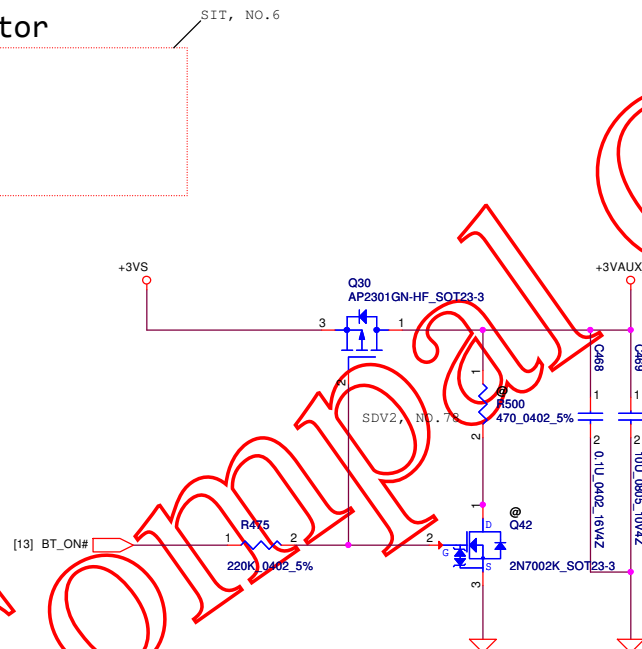
Security Classification	Compal Secret Data
Issued Date	2012/11/22
Deciphered Date	2015/11/22
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Title: EC FNE-KB9012	
Size: Document Number	
Customer: LA-8127P	
Date: Tuesday, March 12, 2013	
Sheet: 31 of 51	

# Fintek Thermal sensor Placed near by APU\_CORE

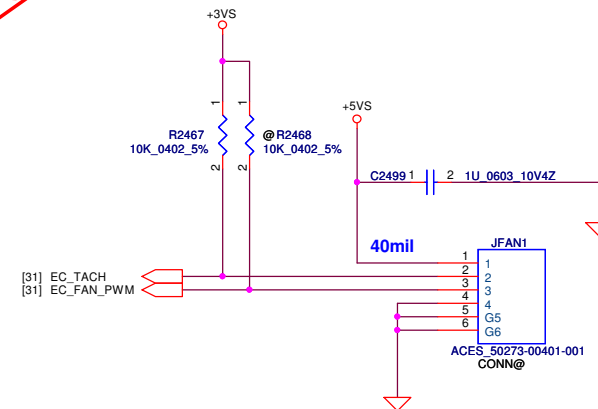


REMOTE1-2+/-:  
Trace width/spa:10/10 mil  
Trace length:<8"

## BT Connector



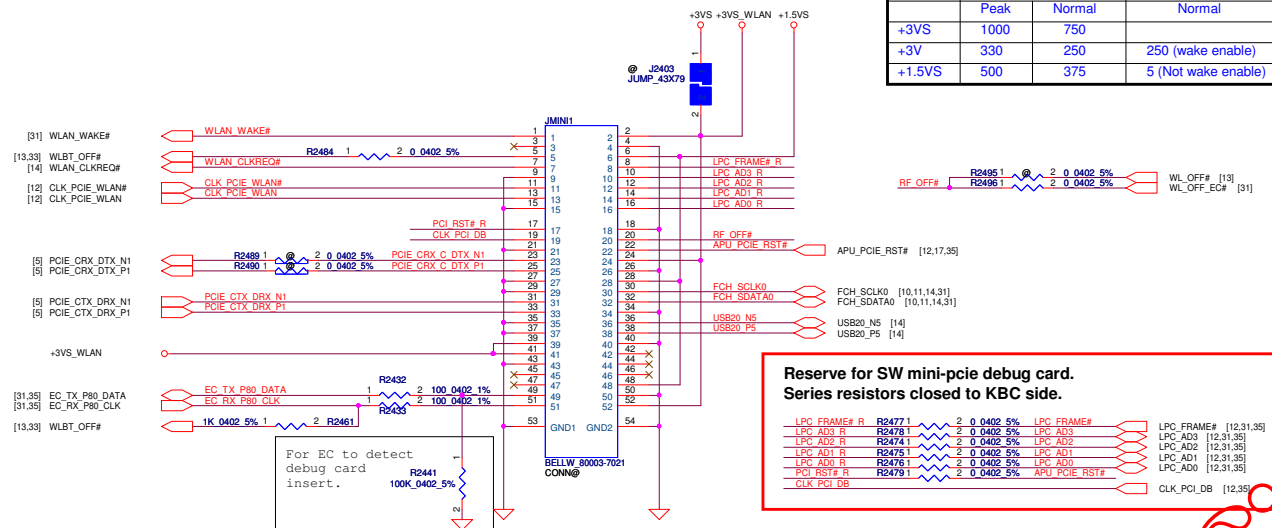
## FAN1 Conn



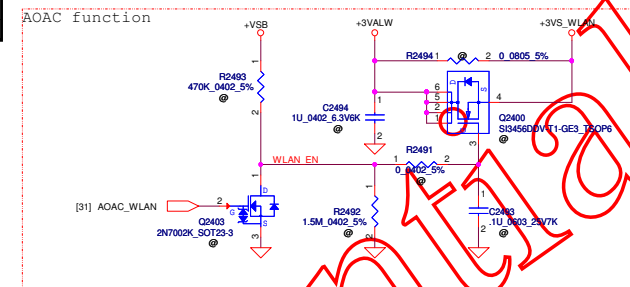
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/11/22	Deciphered Date	2015/11/22	Title	
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				LA-8127P	
				Date	Rev
				Tuesday, March 12, 2013	1.0
				Sheet	32 of 51



## WLAN Conn



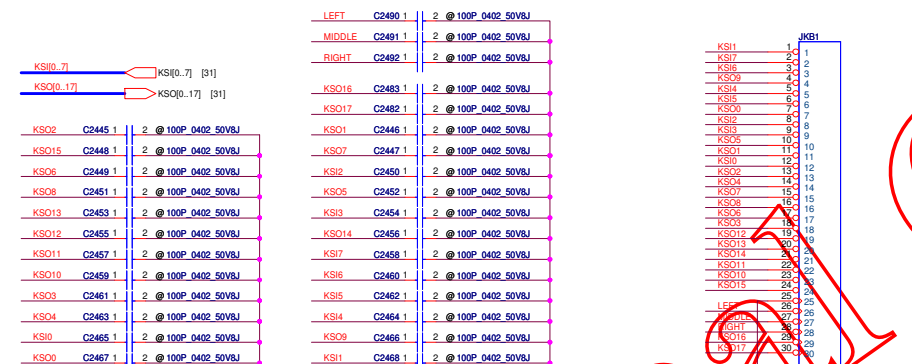
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)



For AOAC assessment

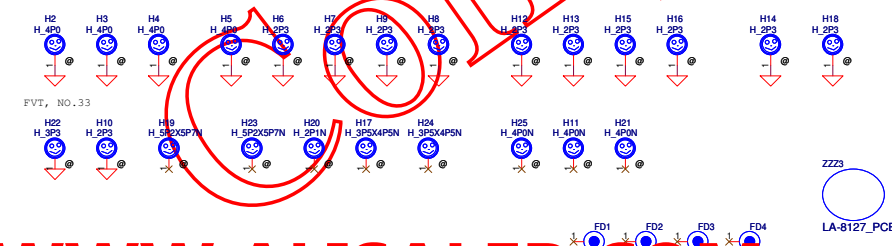
- +3V5 WLAN path:
- 1. +3V5 (default)
- 2. +3VALW
- 3. +3VALW + Switch

INT\_KBD Conn.

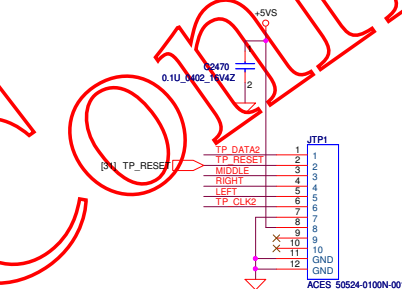


**CONN PIN define need double check**

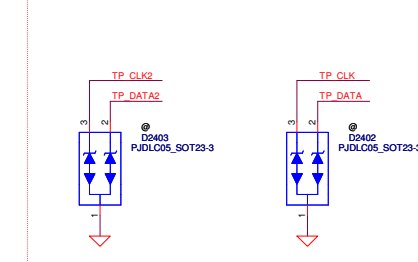
## Screw Holes



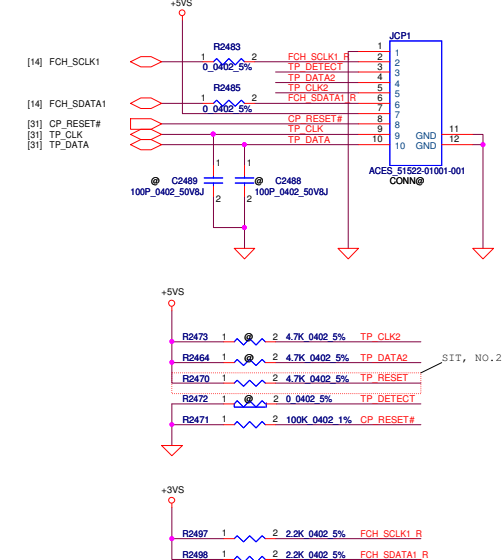
## Track Point Conn



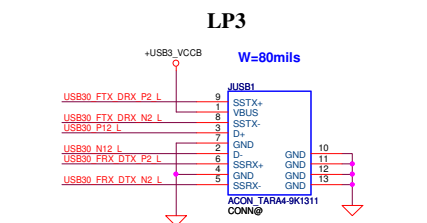
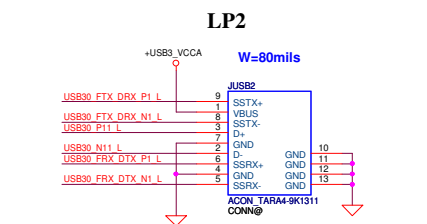
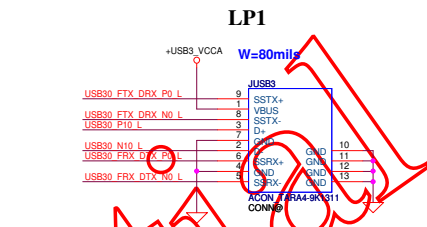
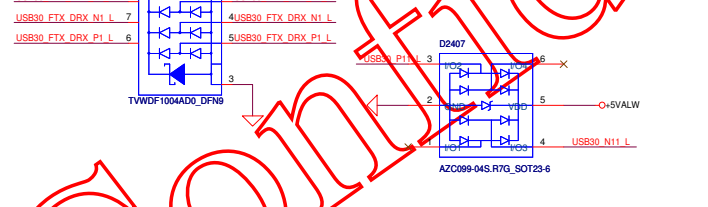
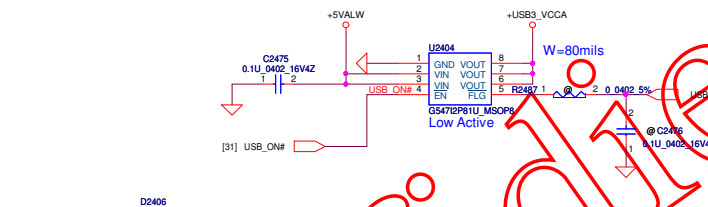
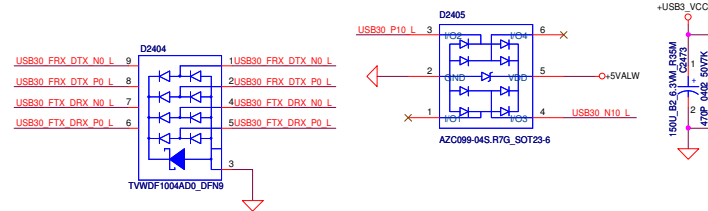
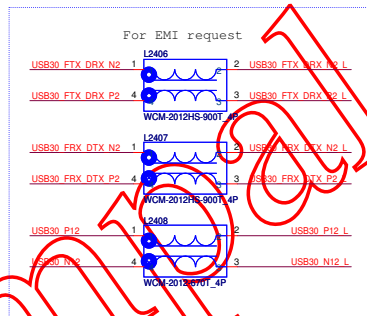
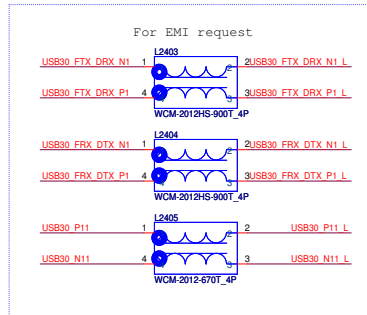
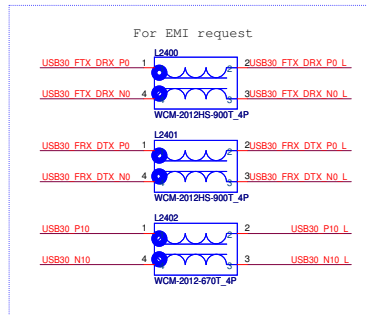
## ESD Request



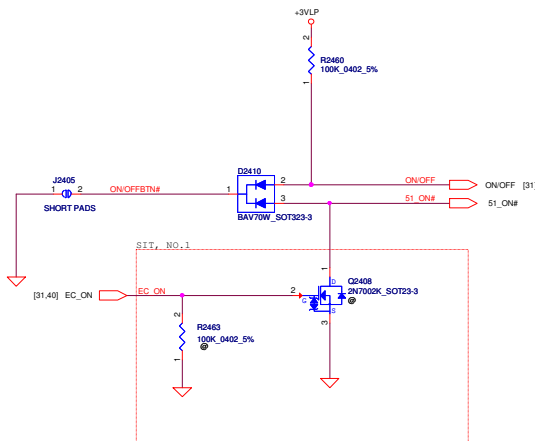
## Click pad 10PIN



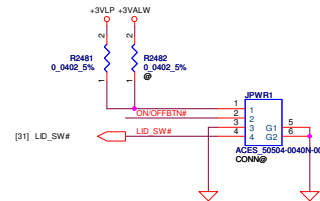
# USB3.0 Conn \*3



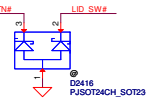
## ON/OFF switch



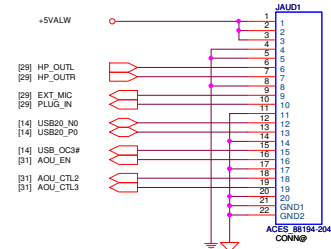
## Power Button Board Conn



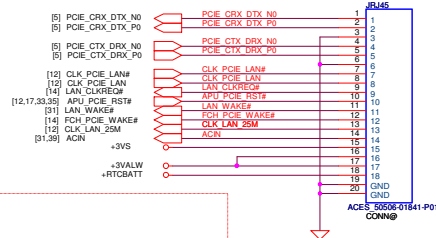
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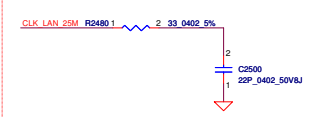
## USB2.0/Audio Jack SB CONN



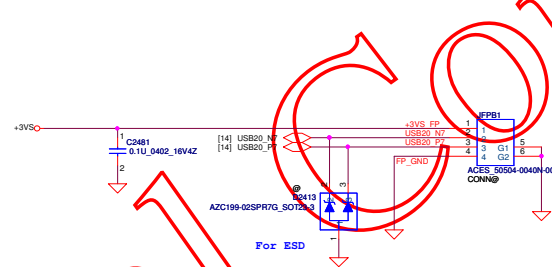
## Lan Conn



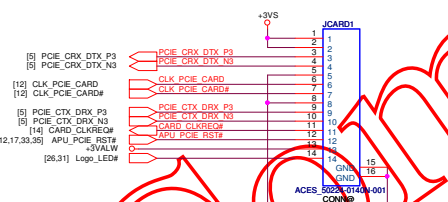
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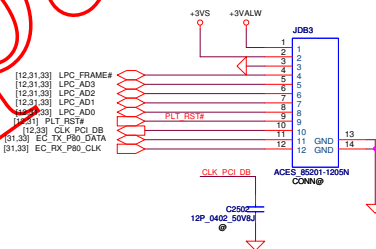
## Finger Printer



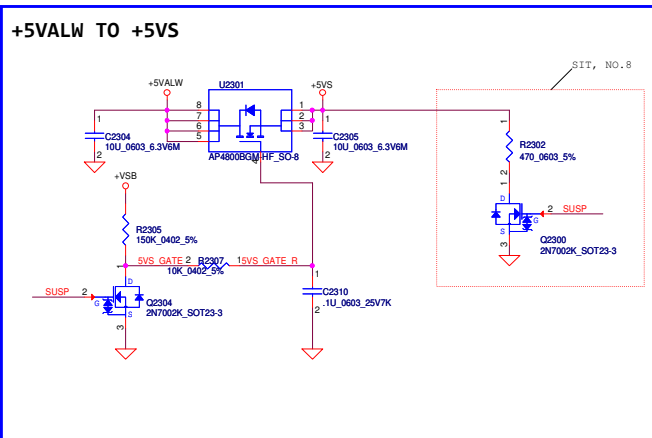
## Card Reader



## Debug Conn



The schematic diagram illustrates a 3V3LW to 3V3S converter. The circuit includes a U2302 MOSFET, a U2303 MOSFET, and a U2304 MOSFET. The 3V3LW input is connected to the gate of U2302. The 3V3S output is connected to the drain of U2302. The 3V3S\_GATE signal is connected to the gate of U2303. The circuit is powered by +VSB and +V3S. A red dashed box highlights the U2303 MOSFET and its associated components, including a 470k resistor and a 2N7002K MOSFET. A label 'SIT, NO. 8' points to the U2303 MOSFET.



### +1.1VALW to +1.1VS

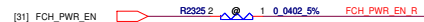
The schematic diagram illustrates the conversion of +1.1VALW to +1.1VS. The circuit features an AP4800BGM-1HF-S0-8 MOSFET driver. The input +VS is connected to the gate of the MOSFET through a 220K resistor (R2315). The MOSFET's source is connected to ground, and its drain is connected to the output of the converter. The output is filtered by a 10V 6315 capacitor (C2314) and a 10V 6315 capacitor (C2315). The output voltage is +1.1VS. A 2SUSP input is also shown connected to the output through a 470 6315 resistor (R2311).

[illegible][illegible]

**+3VALW TO +3V\_FCH**

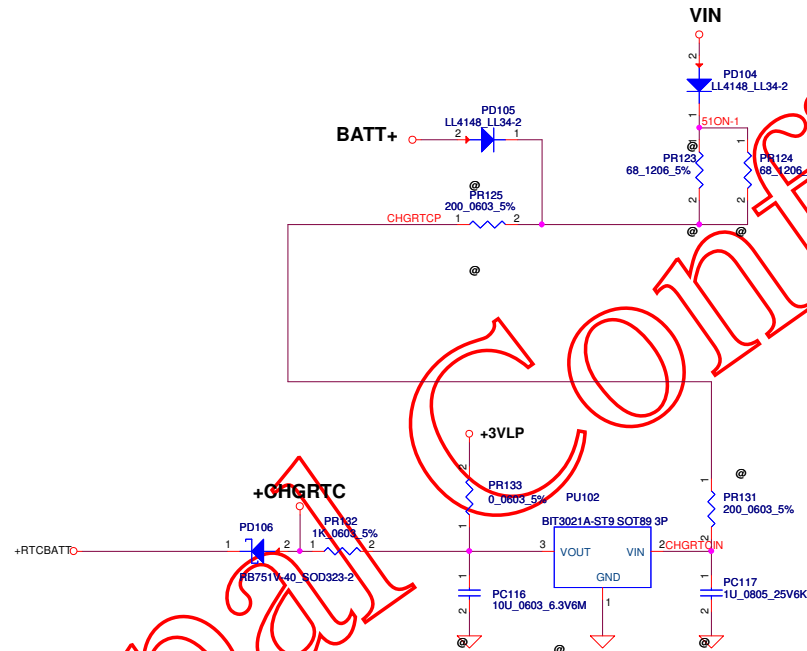
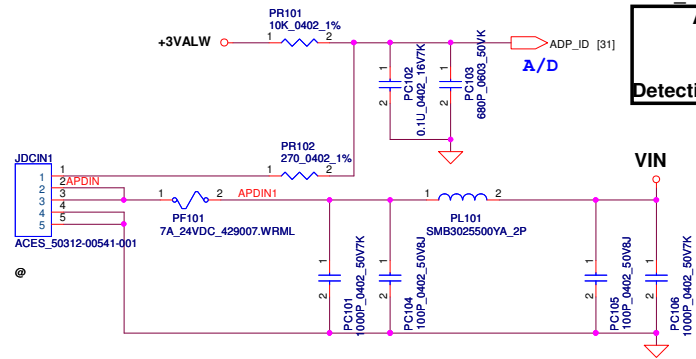
Short J2301 for PCH VCCSUS3.3

The diagram shows a red wire connecting two terminals. The left terminal is labeled +3VALW and the right terminal is labeled +3V\_FCH. Below the wire is a blue component labeled J2301 with a circular symbol and the text JUMP\_43X79 underneath it.



## ADP\_ID

AC Adapter	135W	90W	65W
R(K ohm)	0	open	10
ADP_ID(V)	0	3.3	1.65
Detection voltage	<0.33	>2.64	1.32~1.98



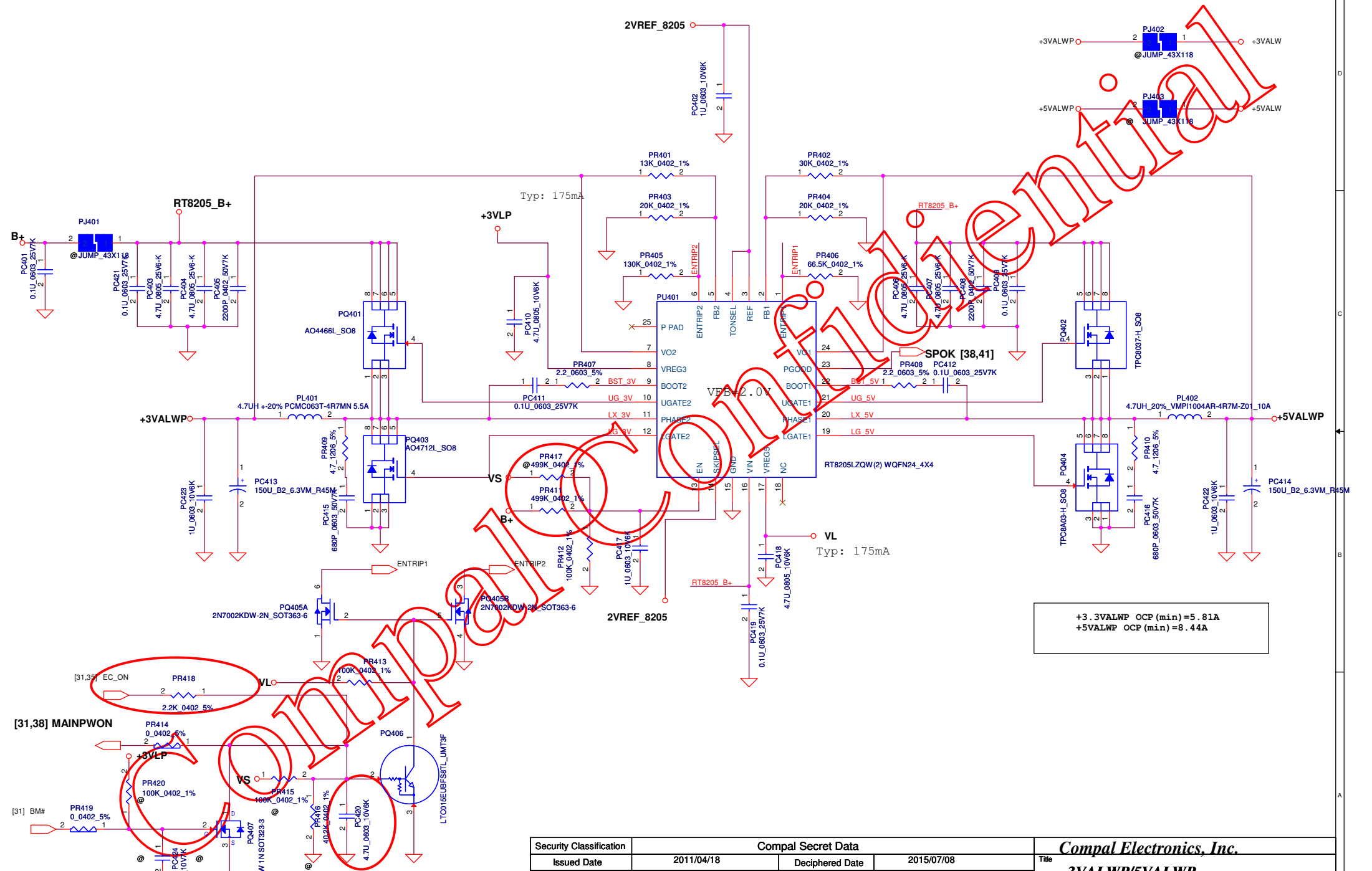
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/04/18	Deciphered Date	2015/07/08	Title	PWR DCIN / Vin Detector /Pre-charge
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				Date: Tuesday, March 12, 2013	Sheet 37 of 51





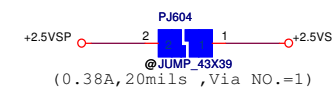
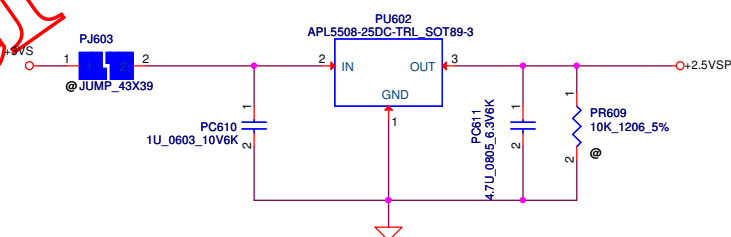
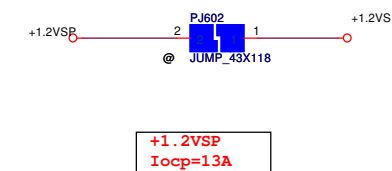
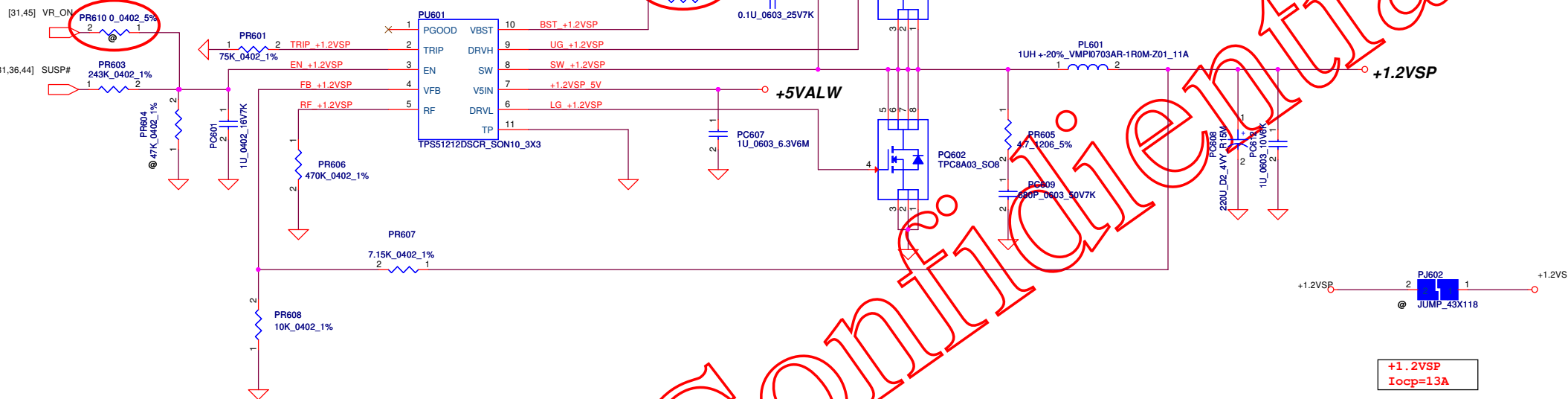


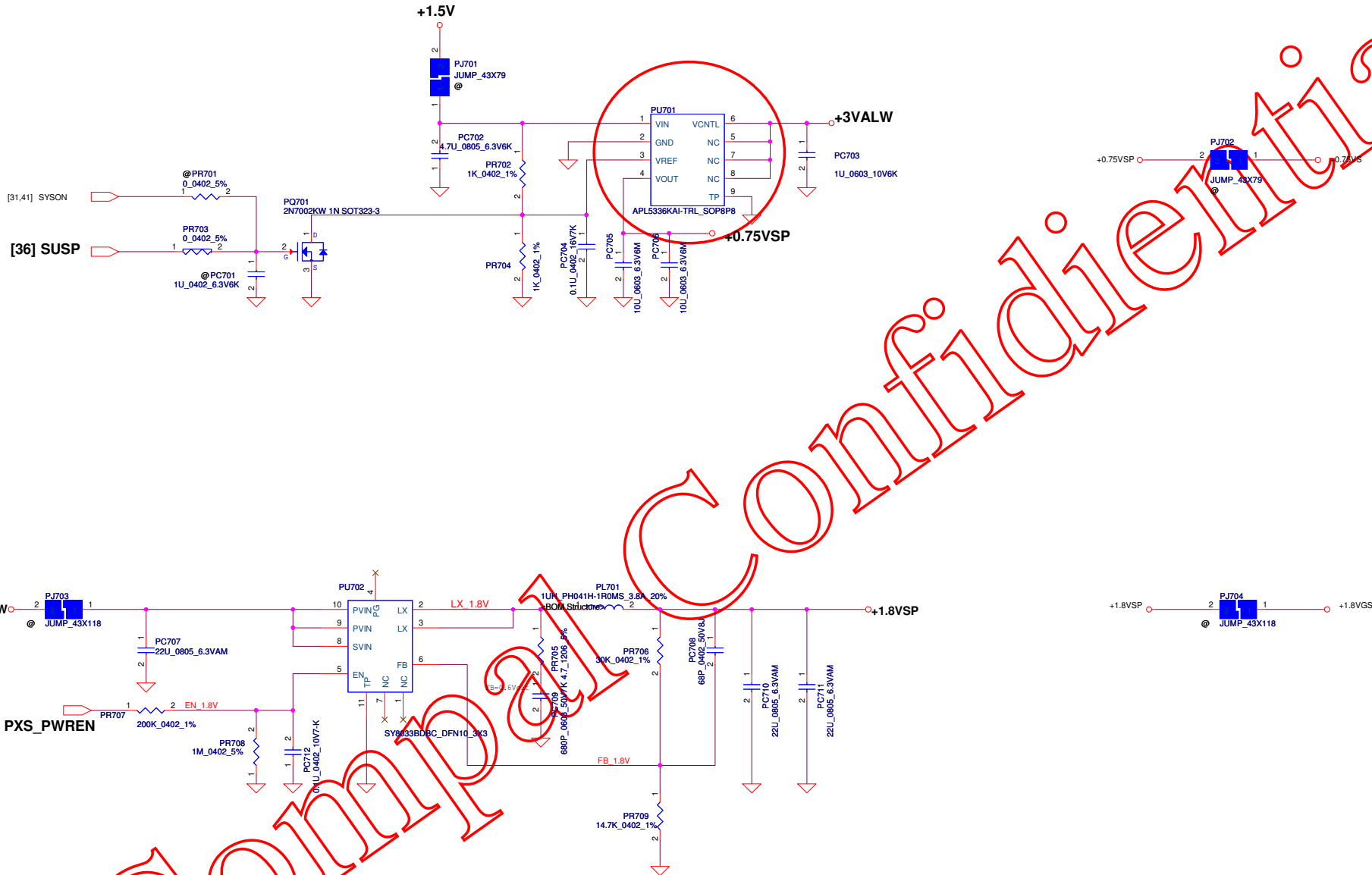
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				Date:	Tuesday, March 12, 2013	Sheet 40 of 51

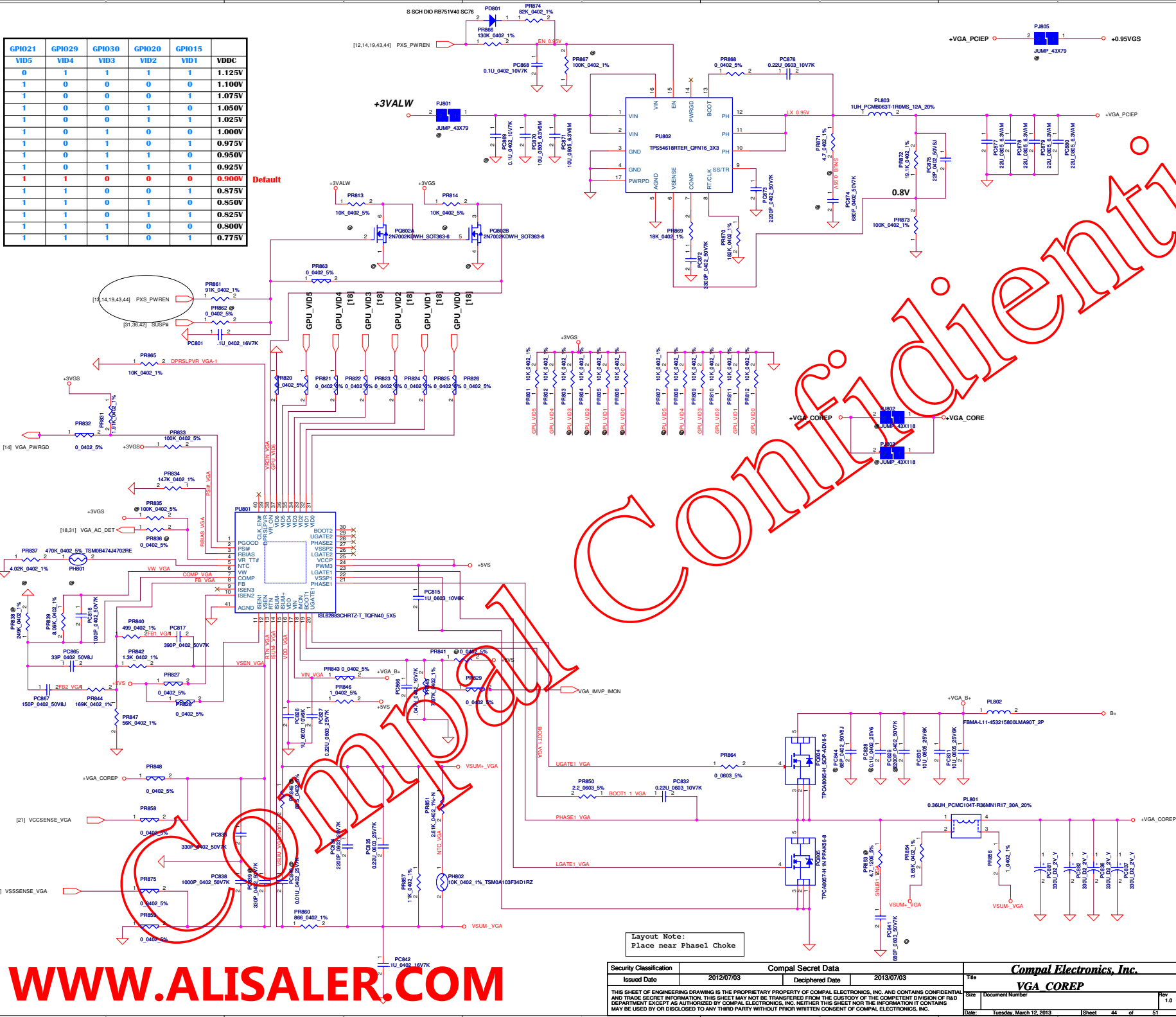






GPIO21	GPIO29	GPIO30	GPIO20	GPIO15	VDDC
VID5	VID4	VID3	VID2	VID1	
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

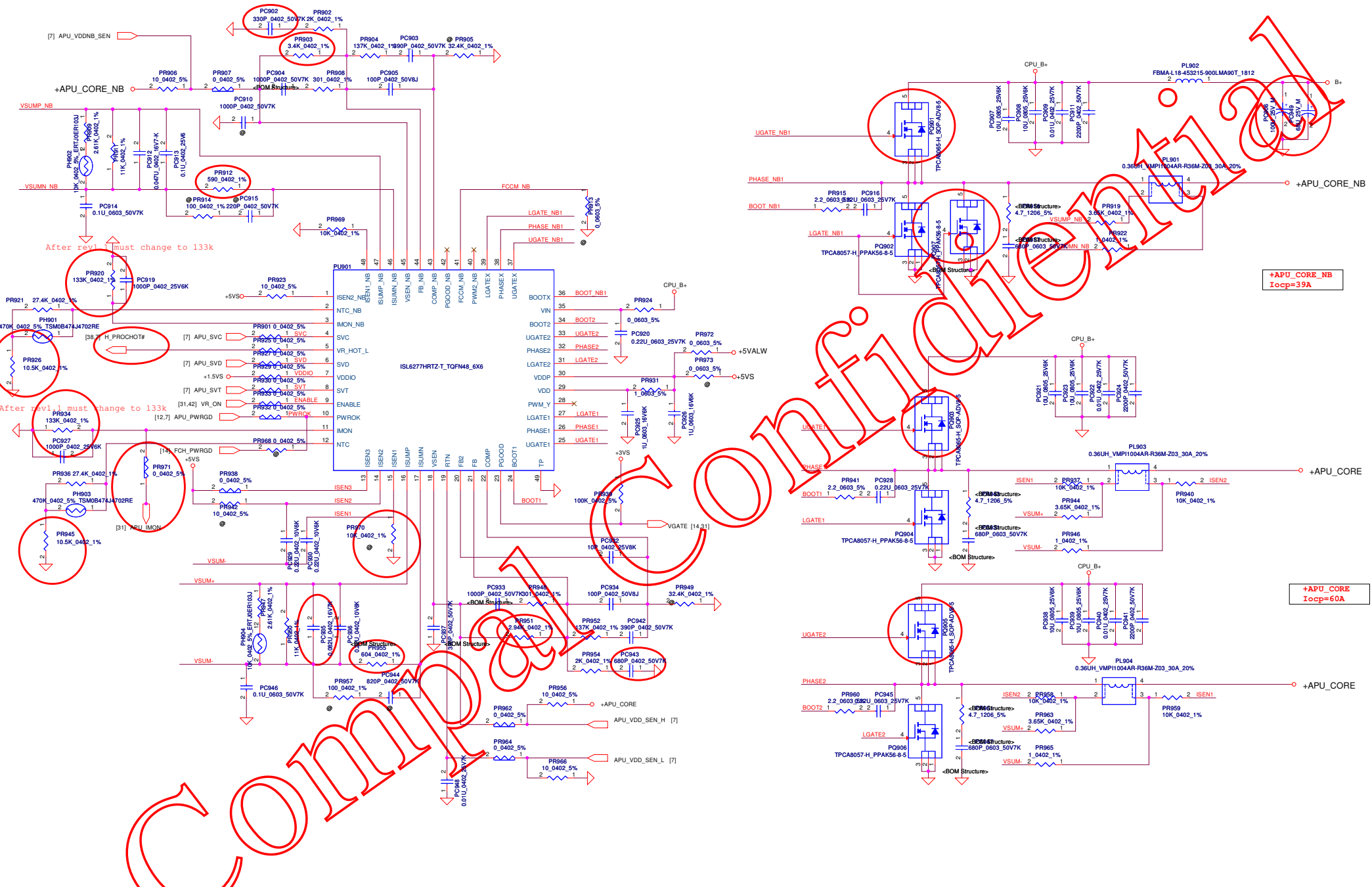


Layout Note:  
Place near Phasel Choke

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Issued Date	Deciphered Date			Doc Number	VGA COREP
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Date	Tuesday, March 12, 2013	Sheet	44	of	51

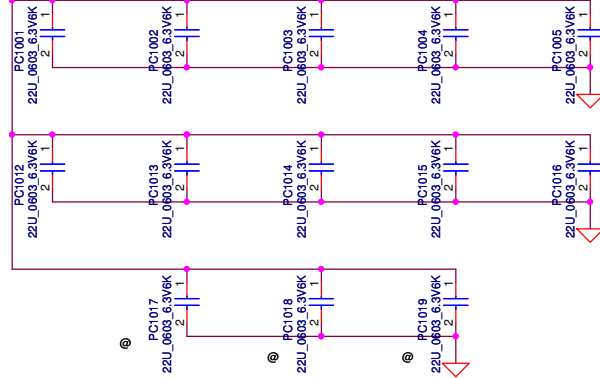
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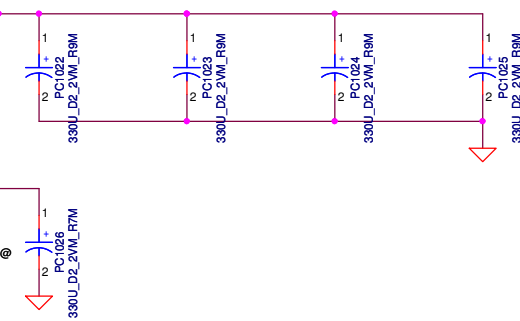
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		CPU COREP	
2011/04/18		2015/07/08		Rev 1.0	
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Date:		Tuesday, March 12, 2015		Sheet 45 of 51	

+APU\_CORE



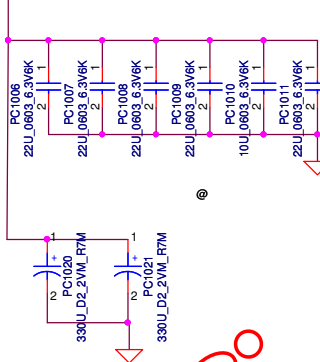
+CPU\_CORE

+APU\_CORE

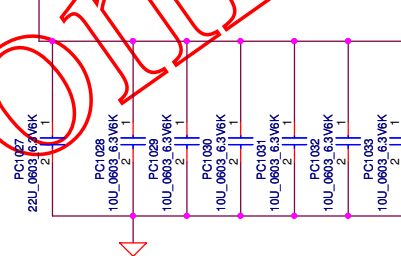


+CPU\_CORE\_NB

+APU\_CORE\_NB



+1.2VS



+1.2VS

## Version change list (P.I.R. List)

Page 1 of 1  
for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Base on EE's request for fine tune power sequence.	P44	Change PR866 from 2.49k to 130k.	2013.1.11	From 0.1 to 0.2
2	For fine tune OCP set up point of VGA core.	P44	Change PR860 from 604ohm to 866ohm.	2013.1.11	From 0.1 to 0.2
3	Base on EE's request for fine tune power sequence.	P44	Change PR861 from 47k to 91k.	2013.1.11	From 0.1 to 0.2
4	Base on must meet EUP spec, change power design.	P37	Remove PR110, PC108, PR114, PC109, PR109, PC107, PU101, PR111, PD101, PR138, PR116, PR112, PD105, PR125, PR128, PC114, PR129, PQ101, PD104, PR123, PR124, PC115, PR131, PC117, PR103, PR104, PR106, PD102, PQ102, PR106, PR107, PQ103, PQ104, PR108, PR118, PR121, PC113, PR127, PQ106, PQ105, PR120, PR115, PC110, PC112, PR126, PR119, PR122, PD103.	2013.1.11	From 0.2 to 0.3
5	Base on must meet EUP spec, change power design.	P39	Remove PQ315, PR328, PR329, PQ316, PD304, PD301, PD302, PQ303, PR303, PR304, PQ306, PC309.	2013.1.11	From 0.2 to 0.3
6	Base on must meet EUP spec, change power design.	P39	Add PR336, PR338, PR337, PR339, PQ319.	2013.1.11	From 0.2 to 0.3
7	Base on must meet EUP spec, change power design.	P40	Remove PR417, PC420, PQ407, PR420, PC424. Add PR411. Change PR418 from 47K to 2.2K.	2013.1.11	From 0.2 to 0.3
8					
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Size		Document Number		Rev	
Custom		C38-G series Chief River Schematic		1.0	
Date		Tuesday, March 12, 2013		Sheet 47 of 51	

Phase	Date	No.	BOM	Sch	Layout	Description
SDV/FVT	2012/11/22	No.1	V	V	V	Page 5, Delete for Sun Pro M2 C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32 Delete PCIE_CRX_GTX_P8~15 PCIE_CTX_C_GRX_P8~15 PCIE_CTX_GRX_P8~15 PCIE_CRX_GTX_N8~15 PCIE_CTX_C_GRX_N8~15 PCIE_CTX_GRX_N8~15
SDV/FVT	2012/11/22	No.2	V	V	V	Page 17, Delete for Sun Pro M2 C1400,C1417,C1418,C1419,C1420,C1421,C1422,C1423,C1424,C1425,C1426,C1427,C1428,C1429,C1430,C1431 Delet PCIE_CRX_C_GTX_P8~15 PCIE_CRX_C_GTX_N8~15
SDV/FVT	2012/11/22	No.3	V	V	V	Page 17 ,U1401 change Part Number from SA000047H50 to SA00006BA30 for Sun Pro M2
SDV/FVT	2012/11/22	No.4	V	V	V	Page 24, Delete for Sun Pro M2 no Channel B C1621,C1622,C1623,C1624,C1625,C1626,C1627,C1628,C1629,C1630,C1631,C1632,C1633,C1634,C1635,R1462,R1463 C1636,C1637,C1638,C1639,C1640,C1641,C1642,C1643,C1644,C1645,C1646,C1647,C1648,C1649,C1650,R1464,R1465 C1651,C1652,C1653,C1654,C1655,C1656,C1657,C1658,C1659,C1660,C1661,C1662,C1663,C1664,C1665,C1569 C1666,C1667,R1504,R1504,R1505,R1505,R1506,R1507,R1508,R1509,R1510,R1510,R1511,R1511,R1512,C1570 R1513,R1514,R1515,R1516,R1517,R1518,R1519,R1520,R1521,R1522,R1523,R1524,R1525,R1526,R1527,U1409,U1410,U1411,U1412
SDV/FVT	2012/11/22	No.5		V	V	Page 19, Reserved T1406,T1407 for Sun Pro M2
SDV/FVT	2012/11/22	No.6	V	V	V	Page 18, Reserved D1401 for Sun Pro M2 PX5.5
SDV/FVT	2012/11/22	No.7	V	V	V	Page 19, Delete PX4.0 and PX5.0 schematic C1459,C1460,C1461,C1462,C1463,D1400,Q1401,Q1402,Q1403A,Q1403B,Q1404,Q1405,Q1406,R1401,R1438,R1439,,R1440, R1442,R1460,R1461,U1402,U1403
SDV/FVT	2012/11/22	No.8	V	V	V	Page 20, Delete DGPU Display Power not need reserved C1472,C1473,C1474,C1475,C1477,C1478,C1479,C1480,C1481,C1482,C1483,C1484,C1487,C1488
SDV/FVT	2012/11/22	No.9	V	V	V	Page 20, L1405 change Part Number from SM010009U00 to SM01000AX00 for Sun Pro M2 Spec Suggetion 120 to 220 ohm
SDV/FVT	2012/11/22	No.10	V	V	V	Page 20, Delete R1457,R1458 ,Because the Sun Pro M2 AW28,AW18 are NC.
SDV/FVT	2012/11/22	No.11	V	V	V	Page 20, Delete Thames&Seymour reserved R1407,R1408,R1409,R1410,R1411,R1412,R1413,R1414,R1415,R1416,R1417,R1466,R1467,R1468,R1469,R1471
SDV/FVT	2013/1/10	No.12	X	V	V	Page 12 U2 change Part Number from SA000066K10 to SA000066K60
SDV/FVT	2013/1/10	No.13		V	V	Page 31, for Power Eulot 6 modfiy Delete net FSTCHG,BATT_LEN#
SDV/FVT	2013/1/11	No.14	X	V	V	Page 18, for fine tune VGA Power saving Stuff C1441
SDV/FVT	2013/1/11	No.15	X	V	V	Page 19, for fine tune VGA Power Sequence R1445 change value from 20K to 470K R1446 change value from 20K to 10K

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				Date: Tuesday, March 12, 2013	Rev 1.0
				Sheet 48	of 51



Phase	Date	No.	BOM	Sch	Layout	Description
SIT	2013/1/10	No.1	v	v	v	Page 35, for Power Eulot 6 modfiy Un-Stuff @ Q2408,R2463
SIT	2013/1/10	No.2	v	v	v	Page 33, for Touch Pad Module requirment Stuff R2470
SIT	2013/2/1	No.3	v	v	v	Page 07, for APU_SID and APU_SIC voltage smothly Stuff C69
SIT	2013/2/1	No.4	v	v	v	Page 26, for Logo LED brightness change Resistor Valve from 4.99K to 1.6K
SIT	2013/2/20	No.5		v	v	Page 36, for delete Discharge circuit ,remove R2324,Q2314,R2321,Q2309
SIT	2013/3/05	No.6		v	v	Page 33, for Factory issue ,remove JBT1
SIT	2013/3/12	No.7	v	v	v	Page 25, for cost down ,not need reserved for EC ,non-stuff Q2107,R2177,R2178
SIT	2013/3/12	No.8	v	v	v	Page 36, for customer request , Stuff R2302,R2303,Q2300,Q2302

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		Tuesday, March 12, 2013		1.0	
		Sheet		49 of 51	

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Size		Document Number			Rev
Customer		LA-8126P			1.0
Date:		Tuesday, March 12, 2013		Sheet	50 of 51





Phase	Date	No.	BOM	Sch	Layout	Description
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				Sheet 51 of 51	